Ascend

October 1996

TECHNICAL OVERVIEW

PASSIVE VS. ACTIVE DESIGNS

ISDN BRI Terminal Adapter Hardware Implementations

ASCEND

TABLE OF CONTENTS

1. INTRODUCTION 1

2. ACTIVE ISDN DESIGN SOLUTIONS 1

HARDWARE DESIGN CONSIDERATIONS 1

Hardware Components 1

Micro-controller 2

Flash EPROM 2

RAM 3

Dual Port SRAM 3

HDLC Controllers 3

ISDN Transceiver and Analog Front-End 3

Bus Interface and Address Decoding Logic 4

SOFTWARE DESIGN CONSIDERATIONS 4

Target System Software 4

Host PC Software 5

3. PASSIVE ISDN DESIGN SOLUTIONS 5

HARDWARE DESIGN CONSIDERATIONS 5

Hardware Components 5

PAL (or ASIC) 7

HDLC Controllers (or ASIC) 7

ISDN Transceiver and Analog Front-End 7

SOFTWARE DESIGN CONSIDERATIONS 7

4. THE NETWARP ISDN SOLUTION 8

© 1996, Ascend Communications, Inc.

1. Introduction

The Integrated Services Digital Network (ISDN) is finally about to come of age in North America. Both service providers and customer premise equipment (CPE) vendors are rushing to make available new products that capitalize on the surge in demand. An unfortunate side effect of this rush to market is that many equipment vendors have not taken the time to seriously consider the pros and cons of choosing a particular implementation approach over another. This paper discusses the two primary implementation approaches for bringing ISDN terminal adapter, internal add-on card, capabilities to the IBM-compatible PC market. These design approaches are sometimes referred to as the "passive" and "active" design solutions. Both of these approaches provide reliable access to the ISDN network but each approach has its own advantages and disadvantages.

2. Active ISDN Design Solutions

A "active" or "intelligent" ISDN terminal adapter is a device which employs native (on-board) intelligence to implement, at a minimum, the ISDN D channel signaling protocols and possibly other B and D channel user protocols. Within the context of a PC add-on card, the active device understands the details of the ISDN interface and can provide services using that interface with little host processor intervention.

HARDWARE DESIGN CONSIDERATIONS

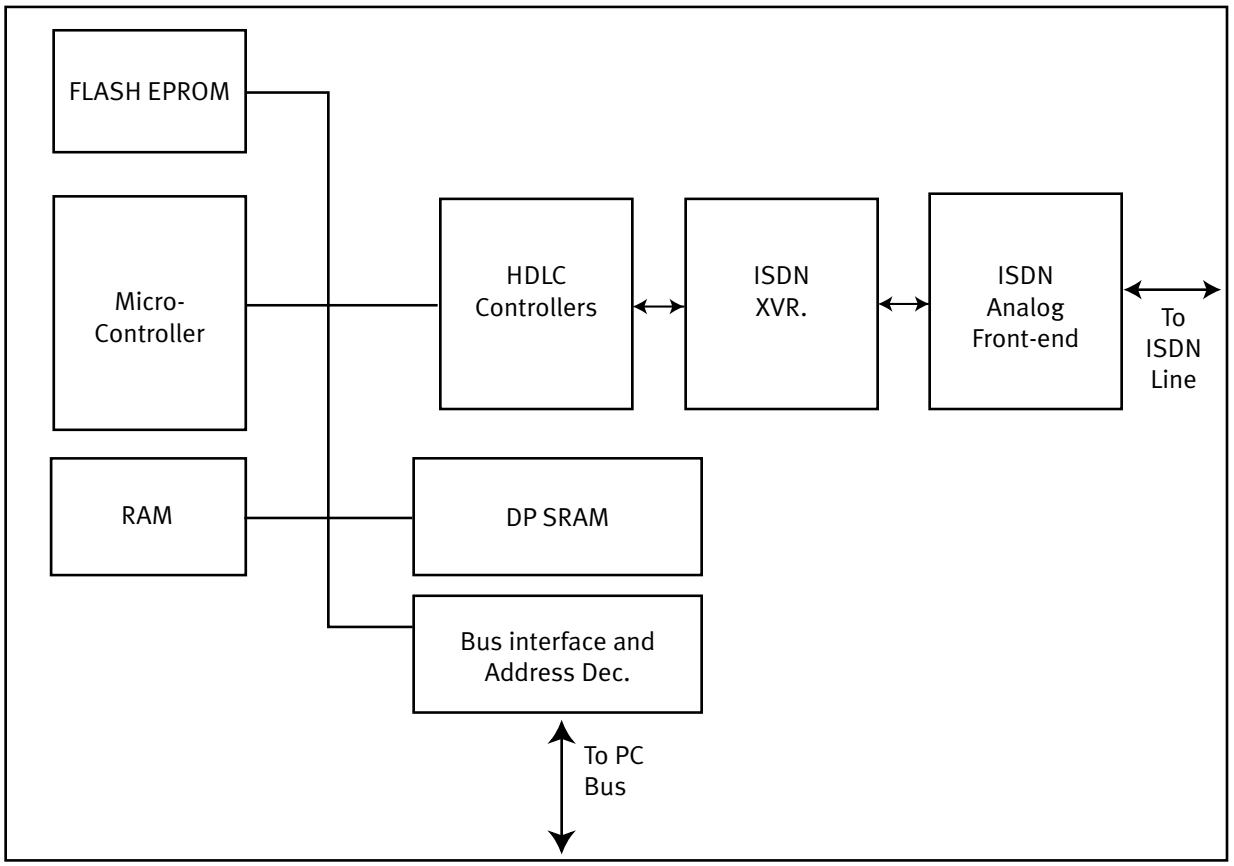
Until quite recently, most ISDN Terminal Adapters (TA) have been designed and developed as active solutions. Stand-alone terminal adapters, as a result of their relative independence from the host processor, have always used active designs. As the ISDN TA has migrated onto the host PC bus, there has been a reluctance to redesign these products to take full advantage of the host PC. Generally, active solutions (when properly designed) offer the potential to reduce load on the host processor and increase flexibility (for features such as analog phone interfaces) with an on-board microprocessor and firmware. This increased flexibility can add substantially to the cost of these products.

Hardware Components

All active hardware designs must provide certain components and the careful choice of these components determines the performance capabilities and cost associated with the design. (Figure 1 illustrates the major components of an active ISDN TA).

© 1996, Ascend Communications, Inc.

Figure 1: ISDN Active Add-on Card Design Components



Micro-controller

The micro-controller is at the heart of an effective, active, ISDN add-on card design. It may incorporate many of the functional units shown in Figure 1 as on-chip peripherals. It should, at minimum, provide a Programmable Interrupt Controller (PIC) and a Programmable Counter / Timer peripheral in addition to the core CPU capabilities. The selection of this micro-controller involves price / performance tradeoffs. Low-cost controllers may need substantial and expensive external peripheral support. Higher-priced controllers may come burdened with more CPU performance and peripherals than are required to accomplish the task. The micro-controller must execute the D channel signaling software and must also transfer B channel data between the HDLC controllers and the Dual Port SRAM. The latter is the most CPU intensive task which the micro-controller must perform, and its interrupt latency is dependent on how much on-chip buffering of B channel data the HDLC controllers can provide.

Flash EPROM

This is where the code and data areas are stored. This area must be large enough to accommodate twice the size of any anticipated modifiable code and data areas. In addition, it must accommodate a stable bootstrap loader which works in conjunction with host software to allow the card to be updated with new firmware. Most ISDN third party software occupies, at minimum, 256K bytes of code space. You can already see that Flash EPROM requirements exceed 512K bytes without accounting for unanticipated bug-fix upgrades and functional enhancements. Flash EPROM can be quite expensive and should be mirrored to guarantee recovery from certain error conditions. If substantial functional or feature improvements are expected, a designer may need to increase EPROM requirements to provide an upgrade capability and to protect against early obsolescence. This can be quite a tricky and potentially costly exercise in prognostication.

© 1996, Ascend Communications, Inc.

RAM

This is where "scratch" data areas used during run-time can be stored. This area can be a part of the DP SRAM or may be DRAM. If one excludes the RAM required for B channel buffer storage, the RAM requirement can range between 16K bytes and 64K bytes.

Dual Port SRAM

Static RAM (SRAM) can be accessed by the host CPU and the on-board micro-controller. Its function is to provide intermediate buffering for B channel data which is moving between the host and the ISDN line. As data is read from the B channel HDLC controllers, it is stored temporarily in this DP SRAM while packets are assembled. The larger the size of this SRAM, the less frequently the host CPU has to be interrupted to transfer data from the card. This minimizes load on the host CPU. However, buffering too much data can have a negative side effect by introducing too much delay between when the data is received from the line and when it is available for processing by the host CPU. If this delay is long, bandwidth on the line will be wasted resulting in less than optimal data transfer performance. It is important to note that although this card is an active design, it does not ensure that optimal performance will be achieved. Ideally, a packet should be moved as soon as it is assembled to ensure optimal turnaround. PPP packets (used for Internet access) are usually 1500 bytes but most designs use a 32K x 8 SRAM to leverage the advantages of using a high-volume part. The DP SRAM may indeed be the only RAM on the board and some of it may be battery backed-up to provide some nonvolatile data storage without the use of expensive Flash EPROM.

HDLC Controllers

The HDLC Controllers are a critical hardware element in most ISDN TA hardware designs. One HDLC controller is always required to provide support for D channel signaling. Pure telephony applications do not require any HDLC formatting capabilities on the B channels, but most data applications do. An ISDN BRI (2B+D) interface used for data therefore requires three HDLC controllers. These controllers provide facilities for framing (flag generation and detection), semantic transparency (bit insertion), and error detection (CRC generation and verification). These are all CPU intensive tasks which require either bit or byte level processing. Some active ISDN implementations choose to use a powerful on-board processor (such as a DSP) to implement the HDLC functions in software, but this approach is unlikely to result in much of a savings since HDLC silicon is quite inexpensive.

The HDLC controller is responsible for providing access to the raw data in a particular channel. This is usually accomplished by the host controller writing to and reading from some temporary storage directly within the HDLC controller device. This storage is usually implemented as a bidirectional FIFO memory. Some HDLC controllers provide as little as four bytes of FIFO storage while others provide as much as 64 bytes. A small FIFO will require much more attention from the on-board CPU to move data to and from the line. However active implementations generally have excess CPU bandwidth available and are therefore willing to use less expensive HDLC controllers with smaller FIFOs. The local CPU must be in a position to service the HDLC controller shortly after it requests service or data received from the line will be lost.

The HDLC controllers must also provide a TDM bus interface which provides access to the ISDN transceiver on the board. Although each of the major ISDN chipset vendors have developed a proprietary TDM bus, their general nature is quite similar (125us/frame) differing only in the implementation of where channels actually reside within the TDM frame and in special maintenance and configuration channel details.

ISDN Transceiver and Analog Front-End

The ISDN transceiver and analog front-end are a matched set of components that provide the direct interface to the ISDN line. The transceiver implements the actual line code and framing while the front end provides transformers and protection circuitry for the line termination. The U and S interfaces are very different physical interfaces and require different transceiver and front-end sets. These devices provide a TDM output which can be used by the HDLC controllers for access to the channels without

© 1996, Ascend Communications, Inc.

the need to understand the details of the ISDN physical interface. The transceiver and front-end should be qualified by a certifying organization (such as Bellcore in the U.S.) to ensure optimal performance under all line conditions.

Bus Interface and Address Decoding Logic

These hardware functions are usually implemented within a programmable logic device or an ASIC. They include access to the PC bus (such as ISA PnP or PCI or PCMCIA) address decoding and chip select generation for the on-board peripherals, interrupt capabilities to and from the host CPU and local bus arbitration.

SOFTWARE DESIGN CONSIDERATIONS

The development of an active ISDN TA does not eliminate the need for host PC software development. A driver, which understands the access details for the card, still has to be developed for the host. In addition to the host driver, target firmware must be developed for the card itself. The only exception to this is the case where the card looks exactly like an asynchronous modem and uses the common PC UART infrastructure. In this case, existing modem drivers may be used to communicate with the card. (For more information on these considerations refer to the Ascend Communications white paper titled ISDN BRI Terminal Adapter Implementations: Com Port Versus Network Card).

Target System Software

An active terminal adapter implementation, the software on the target platform must contain all of the intimate knowledge of the ISDN and its related protocols. Although some statistical information may be transferred to the host PC for viewing, the target software is responsible for all ISDN services such as connection setup and teardown. The target software also coordinates the transfer of data to and from the line via the HDLC controllers. This data is buffered in the on-board RAM until an entire packet (or possibly several packets) has been collected. The target system then interrupts the host processor which transfers the data to the PC's memory. Some more expensive implementations may actually transfer B channel data to the PC without host intervention. This can be accomplished by the use of a DMA controller (either on the PC or on the target hardware platform).

The target software must implement, at minimum, the following functions:

- Connection Manager - Responsible for communication with host
- ISDN L3 - responsible for connection control on the ISDN interface
- ISDN L2 - responsible for reliable transfer of signaling data
- ISDN Physical Interface Driver - responsible for activation and deactivation
- D Channel Driver - responsible for D channel data transfer
- B Channel Driver - responsible for B channel data transfer
- Bootstrap Loader - responsible for firmware updates

In an active implementation, if power is supplied to the card through an external (non-PC based) supply, the software can be designed to continue to provide ISDN services even when the host PC has been turned off. A good example of this is the use of an analog Subscriber Line Interface Circuit (SLIC) to provide external telephone connections. Since the signaling software is resident on the card, an independently powered card may be used to route calls to and from the telephone interface even when the power to the PC has been turned off.

© 1996, Ascend Communications, Inc.

Host PC Software

The host PC that uses an active card may require a driver that understands how to communicate with the card. This driver has been developed to provide services for Microsoft™ Windows™ applications. The driver must facilitate requests from an upper level application to establish connections using the card. The driver must also transfer data (for transmission using the ISDN connection) to and from the card. Since active designs can provide substantial buffering on the card itself as this driver is less sensitive to the poor interrupt performance capabilities that can be experienced by software using Windows. Applications that disable interrupts for lengthy periods rarely results in any loss of data. Some throughput degradation can be experienced when significant amounts of data are left waiting in buffers on the card.

The host software which needs to be developed for an active implementation is in itself not insignificant. An interface which implements the Microsoft NDIS Miniport API, CAPI or a COM port emulation VxD are all significant software development efforts. The actual details of communicating with the card will be simplified since most of the ISDN-specific intelligence is now resident on the card.

3. Passive ISDN Design Solutions

A "passive" ISDN terminal adapter employs only the processing capabilities of the host PC processor to implement the ISDN D-channel signaling protocols. Other B and D channel user protocols. Within the context of a PC add-on card, the passive hardware device understands very little about the details of the ISDN interface. It cannot provide services using that interface without host processor software that is capable of implementing the ISDN protocol standards.

HARDWARE DESIGN CONSIDERATIONS

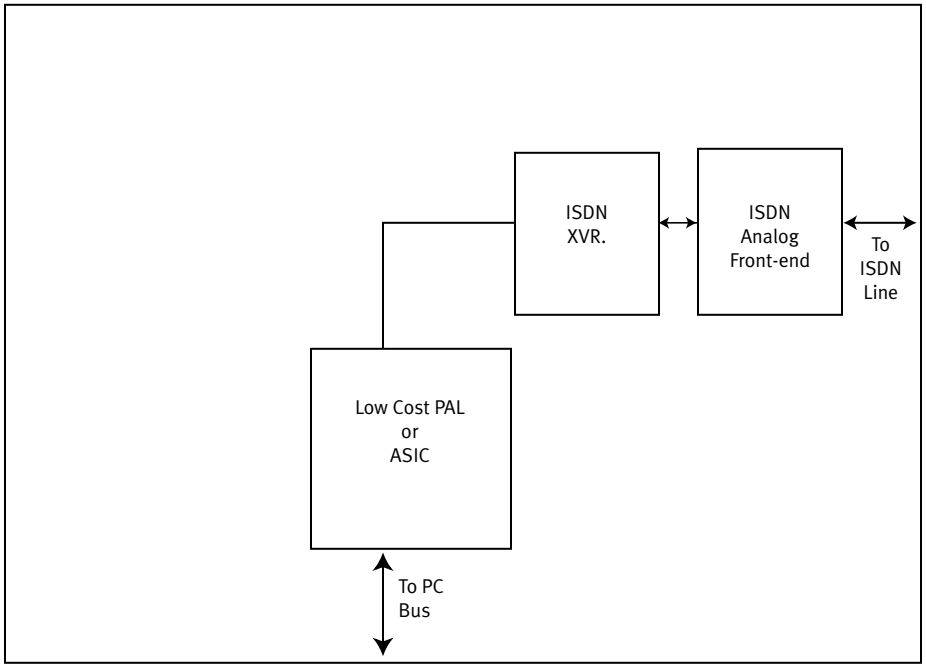
Passive ISDN terminal adapter hardware implementations require careful design consideration to ensure that it provides enough support capabilities to allow the implementation of host ISDN software which will not cripple the host PC processor. The host PC must be able to use the ISDN interface for data transfer, and also retain enough processing bandwidth to support the processing of appropriate application layer software (such as web browsers, and e-mail clients).

Hardware Components

With the use of a very powerful host processor, the minimum passive ISDN TA hardware only needs to provide parallel access to the raw serial data stream for each channel, the ISDN interface transceiver and the analog front-end and termination circuits (see Fig 2). The "Low-cost PAL or ASIC" illustrated in Figure 2 performs all PC bus interface functions. In addition, it would provide minimal data buffering and parallel/serial conversion to and from the TDM interface. The cost of such a device is low for production quantities. However, even the most powerful PC processors available are inadequate to perform all of the processing required to support the ISDN interface while still retaining enough usable bandwidth for host applications.

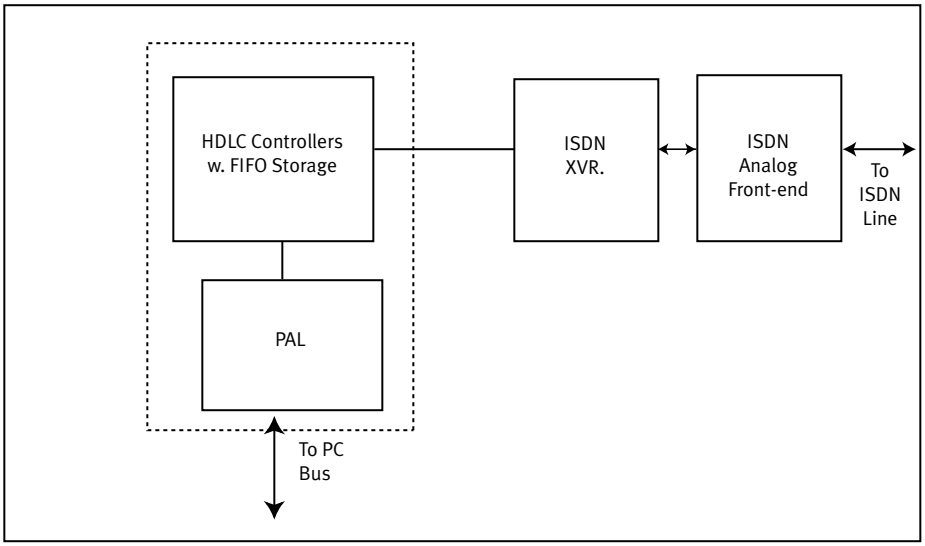
© 1996, Ascend Communications, Inc.

Figure 2: Minimum Passive ISDN Add-on Card Design Components



Current passive ISDN TA implementations seek to ensure a reasonable compromise between maximizing available host processor bandwidth and minimizing the terminal adapter cost. This is most effectively accomplished by introducing hardware support for HDLC formatting for each channel and on-chip FIFO storage capacity to reduce interrupt overhead (see Figure 3).

Figure 3: Current Passive ISDN Add-on Card Design Components



© 1996, Ascend Communications, Inc.

PAL (or ASIC)
This low-cost device provides the PC bus interface capabilities including address decoding, local chip select generation and host interrupts. It allows the host PC to directly access the registers and FIFOs within the HDLC controllers and the ISDN transceiver. This functionality may be combined with the HDLC controller functions within a single ASIC of moderate to low cost.

HDLC Controllers (or ASIC)
The HDLC Controllers in current passive designs provide all of the same capabilities described for those used in active designs. It is critical that these devices provide adequate on-chip FIFO memory storage for buffering data in transit between the line and the host processor. For current PC processors, a minimum of 64 bytes (in each direction) per B channel of FIFO storage should be provided on-chip. The D channel HDLC device requires only 16 bytes (in each direction) of on-chip storage. These devices should be capable of providing an interrupt to the host processor when a completed frame has been received or when the FIFO is partially full (usually using a programmable watermark for maximum flexibility). If the on-chip FIFOs are too small, Windows applications will not be able achieve the minimum response time for servicing a FIFO-full interrupt. The result will be data loss and drastically impaired performance.

Ascend Communications has proved that common, of-the-shelf, general-purpose HDLC controllers, such as those developed by Siemens, are ideal for the ISDN passive application. Ultimately, further cost reductions may be achieved by combining these capabilities with those of the PAL into a single ASIC device of moderate to low cost.

ISDN Transceiver and Analog Front-End
The ISDN transceiver and analog front-end used for a passive ISDN solution provide the same capabilities as those required for an active solution.

SOFTWARE DESIGN CONSIDERATIONS

The development of a passive ISDN TA requires the host driver to implement all of the ISDN protocol intelligence in addition to the physical device handling and upper layer API capabilities.

- The host PC driver software must implement the following functions:
- Upper Layer API - Such as NDIS or CAPI.
- ISDN L3 - responsible for connection control on the ISDN interface
- ISDN L2 - responsible for reliable transfer of signaling data
- ISDN Physical Interface Driver - responsible for activation and deactivation
- D Channel Driver - responsible for D channel data transfer using HDLC controller.
- B Channel Driver - responsible for B channel data transfer using HDLC controllers

One quite significant advantage (aside from the reduced cost) of the passive implementation approach is that the ISDN software can be upgraded simply by installing a new driver on the host PC. This eliminates concerns about capacity for upgrades and providing functional enhancements in the future. The overall result is a substantial extension in the useable lifetime of the product making it a better overall investment.

© 1996, Ascend Communications, Inc.

A possible disadvantage is the fact that the ISDN interface is only usable when the host PC is turned on. Powering the hardware externally does not solve this problem since all of the software intelligence is provided by the host processor. A data user is not likely to see this as a disadvantage since it is unlikely that he or she will be trying to transfer data over their ISDN line without turning on their PC. Nevertheless, analog telephone users need to keep their PC powered if they want to place and accept calls. Many PC users already leave their PCs powered up and depend on the power saving features of the modern PC to reduce the cost when the PC is not in use.

According to most ISDN manufacturers, passive designs will become the dominant TA architecture, notwithstanding the minor disadvantages mentioned above. The passive architecture will allow ISDN terminal adapters to drop below analog modem prices making them the most appealing price/ performance solution available.

4. The NetWarp ISDN Solution

Ascend Communications offers the Netwarp 128 ISDN Terminal Adapter for ISA bus IBM-compatible PCs. The NetWarp adapter is a passive ISDN terminal adapter device and is supported by an NDIS WAN Miniport driver for Windows 95 and NT, and a WinISDN API for Windows 3.1x. The card allows host applications to utilize the full bandwidth of the ISDN BRI for application data transfer providing the maximum performance possible for an ISDN device.

© 1996, Ascend Communications, Inc.



0516

Ascend. Remote Networking Solutions That Work.™

Ascend Communications, Inc.
One Ascend Plaza
1701 Harbor Bay Parkway
Alameda, CA 94502, USA
TEL: 510.769.6001
FAX: 510.814.2300

E-mail: info@ascend.com
Toll Free: 800.621.9578
FAX Server: 415.688.4343
Internet Home Page:
http://www.ascend.com