Lucent Technologies
Bell Labs Innovations

WHITE PAPER

Inverse Multiplexing for ATM

Expanding the Revenue Opportunities for Converged Services over ATM

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1. Introduction

The DS1/DS3 leased line infrastructure installed throughout the Americas over the last several decades created large revenue streams for service providers and changed how enterprises do business. There are many reasons for this huge success. As a digital system based on time division multiplexing (TDM), it provides extremely reliable transport of the highest quality of service (QoS)—even when the highest QoS is not required. The DS1/DS3 infrastructure supports the most demanding real-time applications such as voice, video, and SNA, as well as applications whose requirements are less strict, such as data traffic based on IP and frame relay.

But the DS1/DS3 infrastructure has a significant shortcoming: a large bandwidth gap between DS1 (1.5 Mbps) and DS3 (45 Mbps). This bandwidth gap is due more to an accident of history than to a failure to plan. The relevant standards bodies wrote a third standard—DS2—with an intermediate bandwidth (6.3 Mbps) that was meant to be a convenient stepping stone between DS1 and DS3 link speeds. However, DS2 links were never widely deployed. The result is that enterprises requiring more bandwidth than a single DS1 and less than the much more expensive DS3 have faced awkward and expensive choices.

Standalone inverse multiplexing equipment was developed to address this problem. These inverse multiplexers had multiple DS1 (or other speed) interfaces that connected on the WAN side to multiple parallel leased lines. They also had a higher speed interface that connected on the enterprise side to various types of equipment, for example a PBX, SNA front-end processor (FEP), or router. In short, an inverse multiplexer at each end of the connection aggregated and de-aggregated multiple parallel DS1 leased lines into a single higher speed link. The entire process was transparent to the enterprise equipment, which behaved as if it were using a higher speed link. Although inverse multiplexers were costly, in many cases they were less expensive than paying for a full DS3 leased line that would only be partially utilized.

The ATM Forum, the principal standards body governing ATM, has applied this concept to ATM to come up with the Inverse Multiplexing with ATM (IMA) 1.1 standard. The Forum modified traditional inverse multiplexing somewhat to ensure that the strict QoS guarantees for which ATM is widely known were not disrupted. With this standard, all ATM QoS classes operate reliably over IMA-aggregated links at convenient bandwidth intervals between DS1 and DS3. ATM itself provides highly efficient link utilization through its inherent statistical multiplexing capabilities. Thus IMA provides the best of both worlds, ATM with QoS over traditional T-carrier (DS1/DS3) facilities.

IMA is currently implemented in the CBX 500™ Multiservice WAN Switch, the family of PacketStar™ PSAX Multiservice Multimedia Gateways, and in the family of Stinger™ DSL devices.

This white paper provides a conceptual overview of the operational principles of the IMA standard and explains its critical role in the rapidly growing low-speed ATM converged access marketplace.

Note: The IMA 1.1 standard is available from the ATM Forum at www.atmforum.com.

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2. IMA Operational Principles

The Physical Level

At the physical level, an IMA deployment looks like parallel DS1 lines.

For example, Figure 1 shows a future application of the CBX 500 switch using IMA to provide various speed ATM UNI connections to PacketStar PSAX access devices at three customer sites over multiple parallel DS1s. These virtual links have convenient bandwidths that fall between the readily available DS1 and DS3 link speeds.

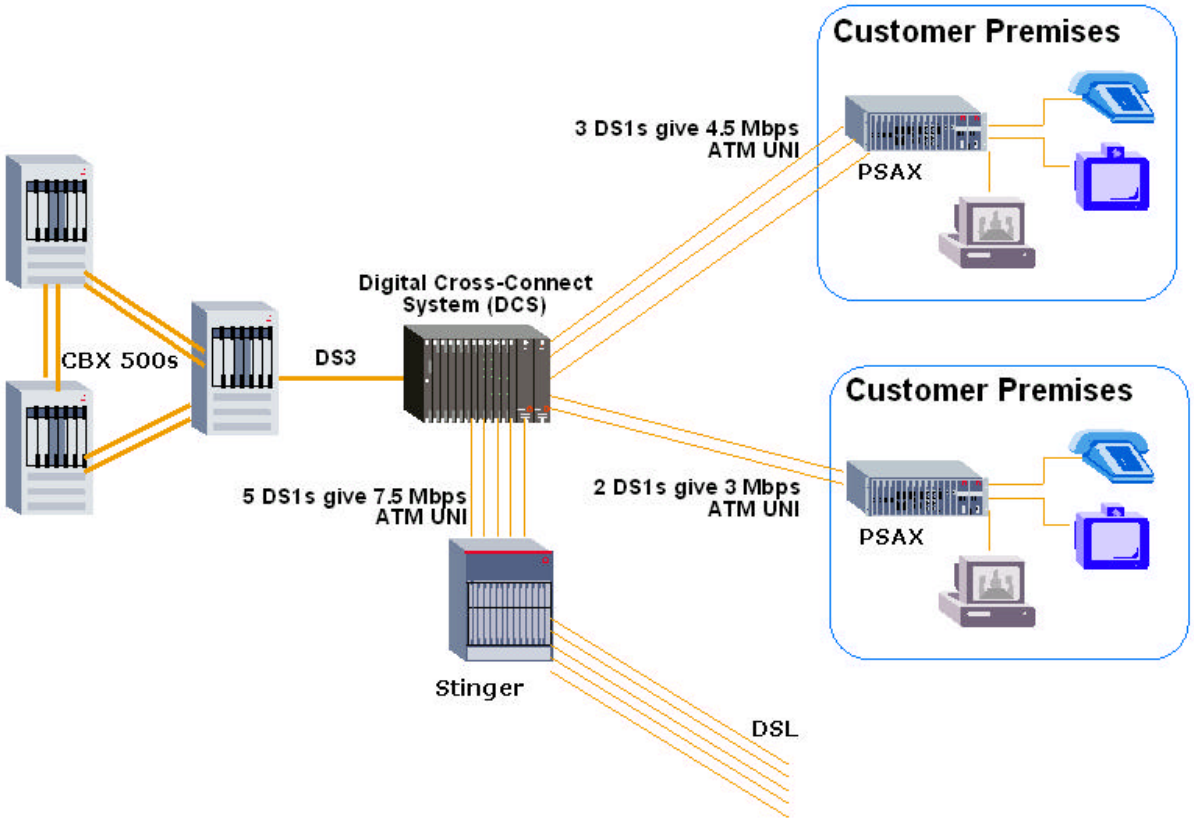

Figure 1 – IMA functionality on the CBX 500 switch, Stinger DSLAM, and the PacketStar PSAX family of access devices enables scalable ATM links in increments of DS1. Such links offer perfect fit, customizable ATM bandwidth that grows as end user needs grow.

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The Logical Level

At the logical level, parallel DS1s bundled together with IMA look like a single physical link that provides the aggregate bandwidth. This virtual high bandwidth link is associated with a UNI (or NNI) interface inside the ATM devices at both ends of the virtual link, just as normal non-IMA links must be associated with a UNI (or an NNI) interface at both ends.

Figure 2 shows the same network as Figure 1, but from the perspective of the higher-level ATM functions—that is, after IMA has unified bundles of parallel physical links into single virtual links.

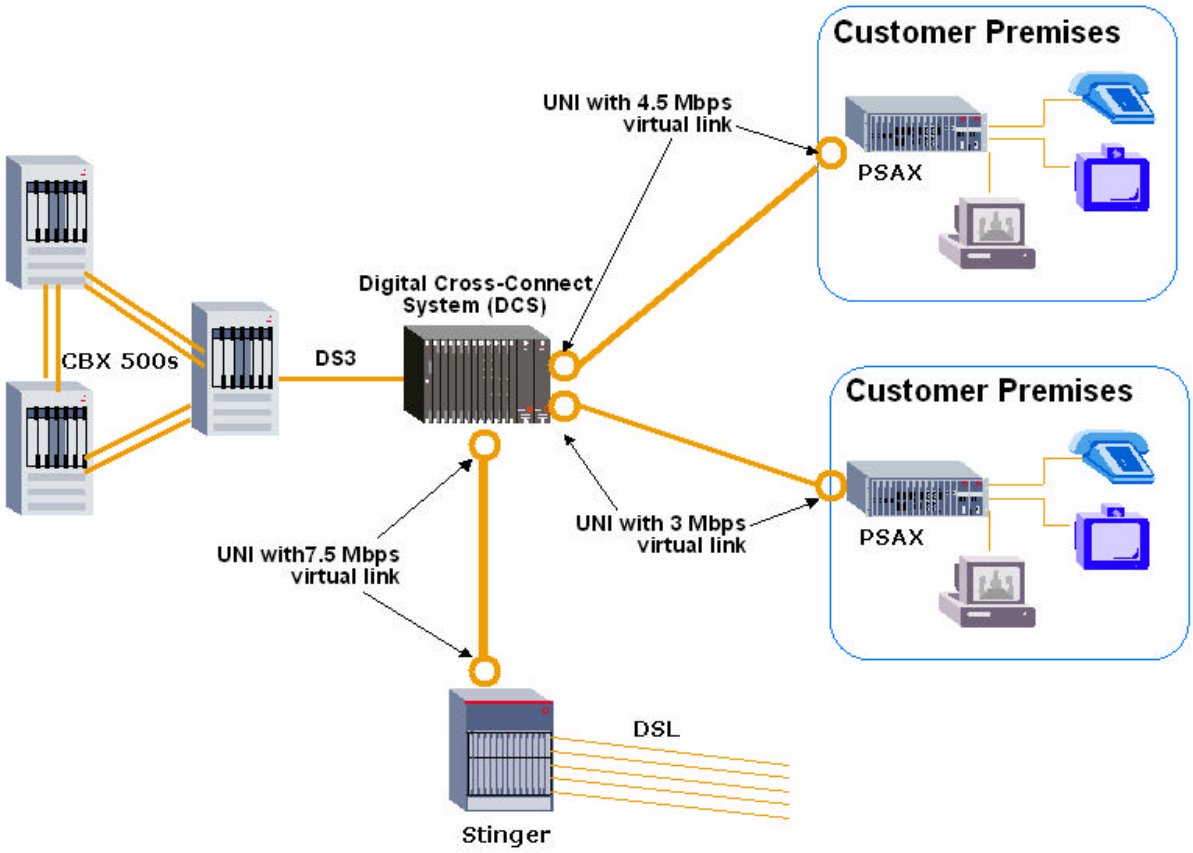

Figure 2—IMA enables a simplified logical view of parallel DS1 lines. A single UNI (or NNI) interface is associated with the IMA virtual link at both ends of the connection. Any configuration that is performed on non-IMA UNIs (or NNIs) can be performed on the UNI associated with the IMA virtual link.

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A Closer Look—Without IMA

ATM networks must maintain cell order when transmitting data. This means that a device receiving ATM cells assumes that they are received in the same order in which they were transmitted. This assumption simplifies ATM transmission significantly while decreasing the need for cell header bits. This approach stands in contrast to many other link layer and network layer protocols in which additional steps must be taken to stitch together frames or packets in the correct order to correctly reconstruct the data stream.

Figure 3 shows how the cell order is preserved when ATM cells are transmitted over a single DS1 link with no IMA. It shows the logical separation between the ATM layer and the physical layer framing. The ATM layer simply transmits cells through its UNI (or NNI) and leaves all framing and other details to the lower level functions, whether IMA is being used or not. Note also that the ATM layer transmits cells at a rate that does not exceed the known rate of the UNI logical port, which in this case is the rate of a single DS1 (1.5 Mbps).

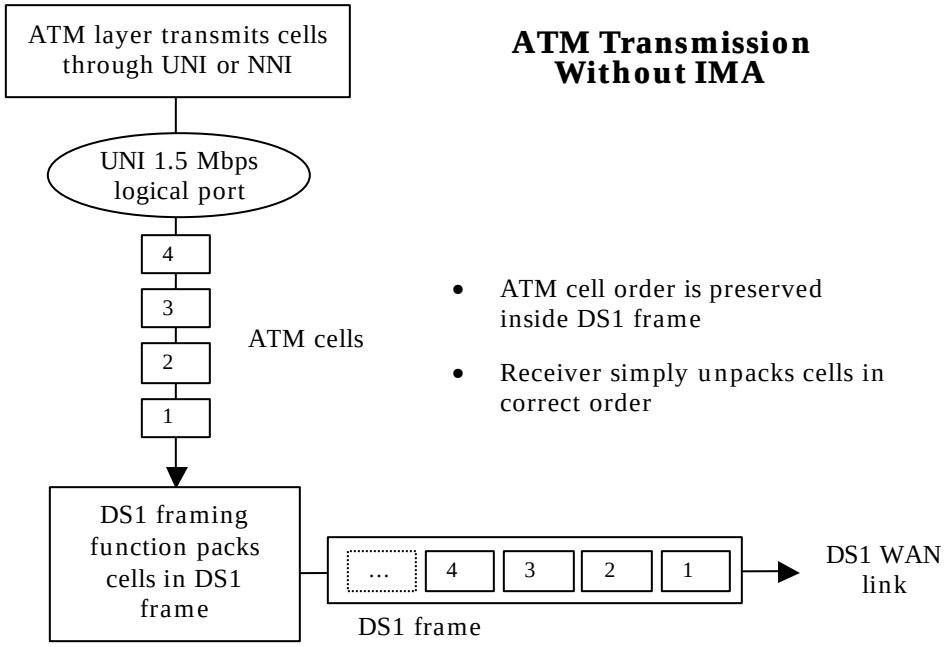

Figure 3—When IMA is not in place, cell order is preserved inside the DS1 frames.

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A Closer Look—With IMA

When IMA is in use, cell order is preserved as shown in Figure 4. IMA receives cells from the ATM layer and distributes them in strict round robin fashion among the DS1 links. This enables the receiving IMA function to reliably reassemble the cell stream from multiple DS1 links.

Figure 4 shows that the ATM layer in the transmitter (or in the receiver for that matter) has no knowledge that IMA is in place. Instead, it simply transmits cells as they are available up to the maximum rate of the UNI logical port—in this case 4.5 Mbps, the aggregate of the three DS1 links.

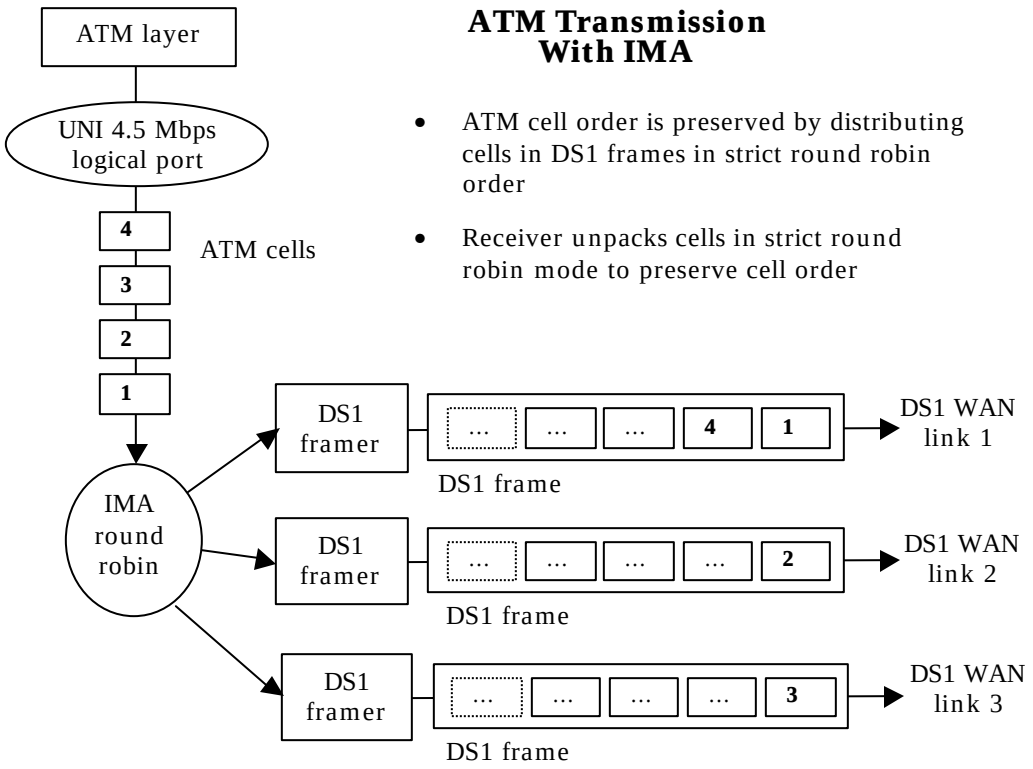

Figure 4—When IMA is in place, cell order is preserved by round robin cell distribution of IMA. Whether IMA is in place or not, the ATM layer has no need to know the details of physical framing.

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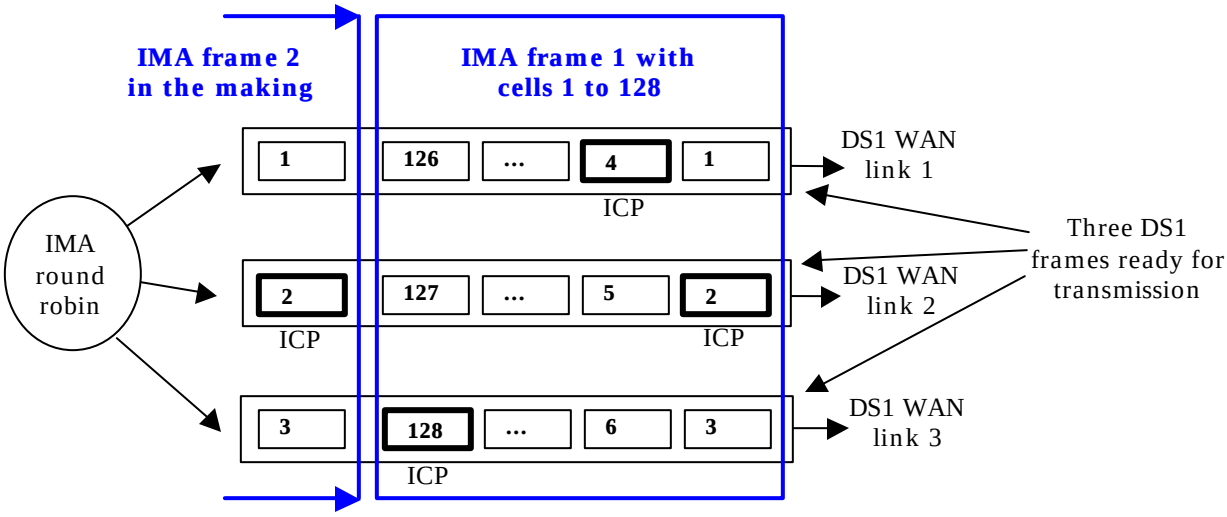
IMA Link Management and Framing

IMA manages a collection of DS1 links to provide a persistent virtual link used to transmit ATM cells in both directions. Individual DS1 links can be added or removed or can fail. The virtual link remains operative at the new bandwidth. Such changes are made on the fly without the need to stop and restart overall traffic flow. These capabilities require additional functionality beyond that discussed so far. What follows is a conceptual overview of IMA frames and IMA Control Protocol (ICP) cells.

An IMA process resides at both ends of an IMA link. The two IMA processes communicate to control data flow and manage the virtual link and its constituent DS1 physical links. Data flow and IMA control communications both occur inside IMA frames. At the simplest level, IMA processes send frames to each other. Each frame contains many ATM cells and a few ATM cells marked as ICP cells. The two IMA processes use ICP cells to communicate and manage everything. A receiving IMA process receives a frame, hands off the data ATM cells to the ATM layer, and uses the ICP cells to manage the whole process.

Each IMA frame is a group of a fixed number of ATM cells (some of which are marked as ICP cells). There are typically 128 cells in each IMA frame, although the frame size can be set to 32, 64, or 256 cells. As cells are handed to the IMA process from the ATM layer for transmission over the WAN, the IMA process distributes them in round robin fashion among the constituent DS1 links. Each IMA frame spans constituent DS1 links, as shown in Figure 5.



Note: The ATM layer, the UNI, and the DS1 framers have been removed from this diagram for clarity.

Figure 5—IMA frames span the DS1 links that make up the virtual link. An ICP control cell is sent once per IMA frame on each DS1 link. The ICP location is always the same on a given DS1 link but differs among DS1 links.

ICP cells are identified by a special code in the cell header and perform important functions in IMA. For example, ICP cells are used by the IMA processes at both ends to communicate the status of the IMA virtual links as a whole, as well as the status of individual DS1 links. ICP cells are used to remove and restore failed and recovered DS1 links from the virtual link. ICP cells are used for other functions too. An ICP cell is transmitted on each DS1 link once per IMA frame. On a given DS1 link, the ICP cell is always in the same location—for example, the fourth cell in the IMA frame, or the 12th cell in the frame. ICP cells can be in different locations on different DS1s. Figure 5 shows that DS1 WAN link 1 always has its ICP cell in the second cell of the IMA frame, DS1 WAN link 2 in the first cell of the IMA frame, and DS1 WAN link 3 in the last cell. ICP cells are shown as bolded cell boxes.

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The non-ICP cells are either ATM traffic cells or idle cells. Idle cells are transmitted only when there is no ATM cell ready to transmit, that is, when the cell rate offered by the ATM layer for transmission over the WAN is less than the virtual link cell rate. This use of idle cells is known as "cell rate decoupling" because the WAN transmits cells at full speed even when the real ATM cell traffic is at a lower speed; the two rates are "decoupled."

Because ICP cells are inserted on each DS1 link once per frame, the IMA process can introduce some delay in the cell flow. However, the standard includes smoothing buffers that remove the delay and allow for virtual circuits of all QoS classes, including those requiring minimal cell delay and predictable cell delay variation. IMA includes bit stuffing and other techniques as well that allow predictable cell delay variation even when the different DS1 links use different clocks and have differential delay variation.

3. IMA on the CBX 500

The CBX 500 Multiservice WAN Switch supports built-in IMA 1.1 on the 3-Port Channelized DS3/1 ATM with IMA I/O module. This I/O module provides the highest ATM DS1 port density per rack in the market. The I/O module has three DS3 interfaces that are channelized to the DS1 level. Each of the three channelized DS3 interfaces supports 28 IMA-enabled DS1s, for a total of 84 DS1s per I/O module. The CBX 500 switch supports 14 I/O modules, for a total of 1,176 IMA-enabled DS1s per switch. A standard telco rack holds two CBX 500 switches for an unprecedented 2,352 IMA enabled DS1 ports per rack.

The 28 DS1s on each physical DS3 port are accessed with a standard digital cross connect device. This device simply breaks out the channelized DS1 lines from the unified DS3 line. This system allows extremely high DS1 port density from the CBX 500 switch.

This I/O module allows you to create IMA virtual links from two to eight DS1s, providing the following incremental bandwidths shown in this table.

Bandwidth	**Description**
1.5 Mbps	no IMA, one DS1
3 Mbps	IMA, two DS1s
4.5 Mbps	IMA, three DS1s
6 Mbps	IMA, four DS1s
7.5 Mbps	IMA, five DS1s
9 Mbps	IMA, six DS1s
10.5 Mbps	IMA, seven DS1s
12 Mbps	IMA, eight DS1s

The high DS1 port density offered by this industry leading I/O module combined with IMA support opens the door to new service provider revenue streams in the rapidly expanding ATM converged access market.

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4. Conclusion

The ATM-IMA Converged Access Synergy

Together IMA and ATM open an important new market opportunity for service providers to offer low-speed converged access over ATM. Service providers can now offer their enterprise customers converged voice, video, and data services over low-speed ATM access lines between 1.5 Mbps and 45 Mbps. This market is poised for significant growth.

Low-speed ATM refers to access links with speeds below DS3 (45 Mbps). IMA opens up this previously expensive and inaccessible bandwidth range. IMA enables the perfect-fit, customizable bandwidth that meets today's ever-expanding throughput needs within the existing DS1/DS3 infrastructure. Remote offices can start with DS1 and increase that bandwidth with ease. Offices that need higher bandwidth can start at any of the IMA increments, without having to pay the high cost of a full—and underutilized—DS3.

Converged access over ATM uses the inherent strengths of ATM to simplify enterprise WAN access. By converging all WAN access needs (voice, video, SNA, LAN, frame relay, ATM, data, etc.) onto a single access method (ATM), service providers can offer a single integrated bill to the customer. This is also known as "one pipe, one bill provisioning."

To equip providers to flourish in this market, Lucent has implemented IMA in the PacketStar PSAX family of Multiservice Media Gateways and on the CBX 500 Multiservice WAN Switch. The combination allows service providers to deploy IMA in the network core, concentration, or access point. Lucent has also extended this capability by adding IMA support to the Stinger™ DSL access platform. ATM is the common thread that binds the wide range of services, technologies, and devices together.

Through its spectrum of quality of service (QoS) guarantees, ATM supports each customer application appropriately—and transparently. For example, traditional PBX connectivity and point-to-point or multidrop SNA is supported transparently with ATM circuit emulation over Constant Bit Rate (CBR) circuits. Videoconferencing is supported with ATM real time-Variable Bit Rate (rt-VBR) point-to-point or point-to-multipoint circuits. LAN and other data applications such as Internet access are supported with Available Bit Rate/Unspecified Bit Rate (ABR/UBR) circuits, or with higher quality circuits as appropriate for service differentiation. Frame relay access devices use the converged access service as well through Lucent's industry leading standards-based frame relay to ATM network and service interworking features. And all of this is transparent to the end user who does not have to grapple with ATM at all—they simply plug existing equipment into one of the diverse user side interfaces of the PSAX access device.

In short, the user of a converged access service connects existing equipment with legacy interfaces and protocols to the converged access switch. The customer has no need for multiple WAN services offering only static bandwidth and inefficient QoS support. Instead, the customer has a single WAN service with dynamic bandwidth and a spectrum of efficient QoS support. This amounts to significant operational and technical simplification. The savings in equipment, in training, and in avoided network downtime far exceed the costs. That synergy streamlines business and increases productivity—which is why the low-speed converged access using ATM market is poised for rapid growth.

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Appendix: The Lucent Solution

The IMA capabilities described in this paper are available on the Lucent CBX 500 Multiservice WAN switch and on the PacketStar PSAX Multiservice Media Gateways.

CBX 500 Multiservice WAN Switch

The CBX 500 Multiservice WAN Switch is a foundation for next-generation networks that service providers use to scale, simplify, and consolidate converged public networks of today and tomorrow. Service providers leverage this switch's intelligence, reliability, and multiservice port density into new revenue sources while streamlining their networks. Deployed at the network core or edge, the 5 Gbps CBX 500 delivers ATM, frame relay, and IP/MPLS carrier-class networking over market leading port densities of fiber optic and electrical interfaces. The quad-plane redundant switch fabric, the output-buffering scheme, and the hardware implementation of ATM service classes ensure end-to-end quality of service (QoS).

PacketStar PSAX Multiservice Media Gateway Family

The PacketStar PSAX Multiservice Media Gateway family works with the GX 550™, CBX 500, and the B-STDX 8000/9000™ Multiservice WAN Switches to equip service providers to respond to customers' growing application and bandwidth needs with a rich portfolio of broadband services for data, voice, and video. PSAX products deliver affordable, broadband access and aggregation on one platform at the customer site or central office. They offer sophisticated quality of service (QoS) management, unparalleled service support, high granularity and scalability, and simple, effective management. The versatile PSAX family is divided into two groups: Central Office, which includes the PSAX 2300 and PSAX 1250; and Customer Premises, which includes the PSAX 600, PSAX 100, PSAX 50, and PSAX 15. Both groups have a modular hardware and software architecture that benefits service providers through significant savings in operational and administrative costs.

Stinger DSL Access Concentrator

Stinger is a new carrier-class DSLAM designed for forward-looking service providers. it supports ATM and frame relay communication protocols, and all of the most common DSL access technologies.

Stinger offers all the benefits ATM brings to multiservice networks—including reduced installation, operation, and maintenance costs; efficient bandwidth management; and high availability.

Addressing the needs of carriers implementing cell-based backbone networks, Stinger features the high-capacity traffic aggregation capabilities and robust always-on performance expected of a true carrier-class product. It offers faster throughput and lower cost per port than any competing product.

About Lucent

Headquartered in Murray Hill, New Jersey, USA, Lucent Technologies designs and delivers the systems, software, silicon, and services for next-generation communications networks for service providers and enterprises. Backed by the research and development of Bell Labs, Lucent focuses on high-growth areas such as broadband and mobile Internet infrastructure; communications software; communications semiconductors and optoelectronics; Web-based enterprise solutions that link private and public networks; and professional network design and consulting services. For more information on Lucent Technologies, visit its Web site at http://www.lucent.com.

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