OPTi®

82C916

Serial Codec

Data Book

912-3000-039
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March 10, 1997

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Table of Contents

Table of Contents (cont.)

List of Figures

List of Tables

Serial Codec

1.0 Features

- Integrated sigma-delta audio stereo codec
- MPC-compatible six stereo channel mixer
- Variable Sample Frequency generator
- Programmable gain and attenuation
- Sample rates from 3.9KHz to 48KHz
- High speed serial interface
- Packaged in a 28-pin Small Outline Package (SOP, 300mm)

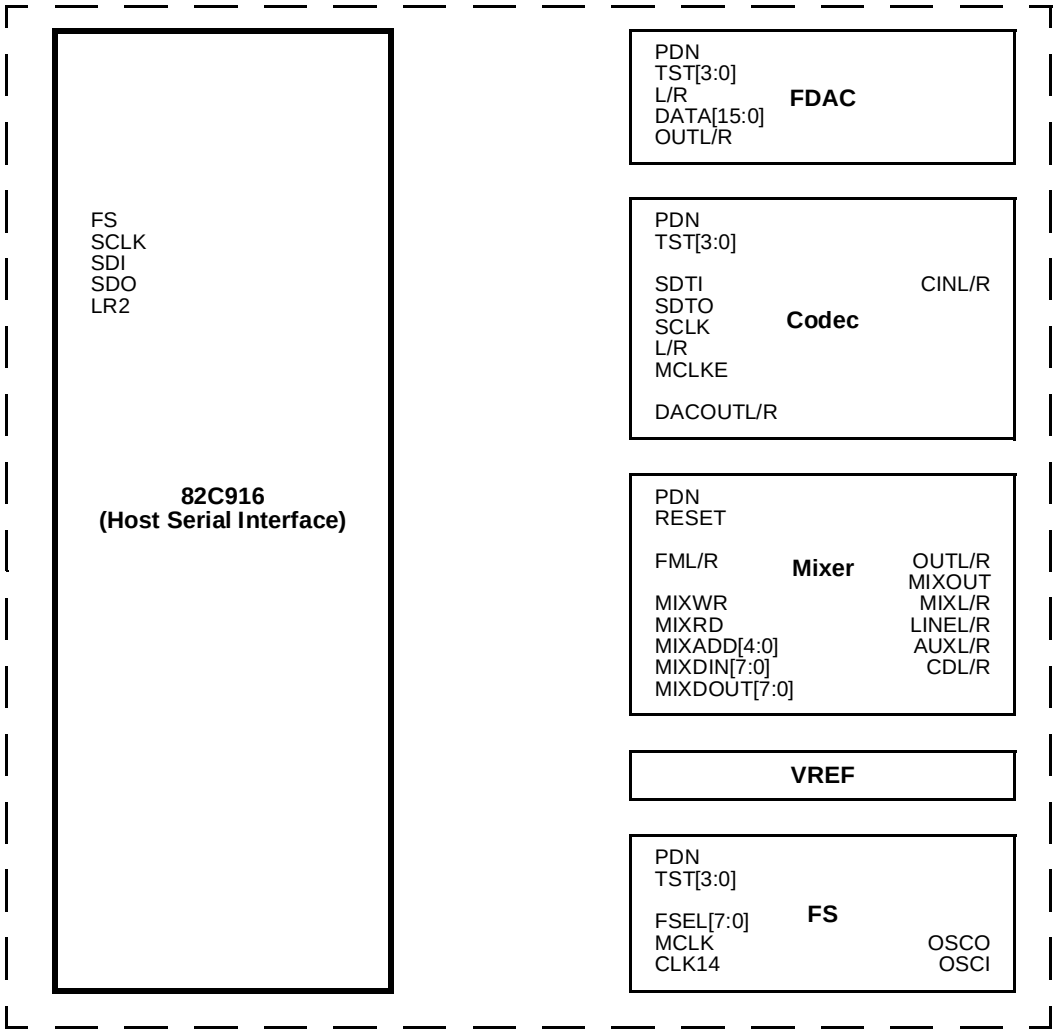
2.0 Overview

The 82C916 is an integrated serial codec for PC audio application. The codec includes stereo audio converters, MPC Level-3 compliant analog mixing, variable sample frequency generator, and support for advanced power-down modes.

The 82C916 provides the integrated solution for the following applications:

- 16-bit sound quality Sound Blaster™ + Windows Sound System™ Compatible Card
- 16-bit CD-quality wave audio up to 44.1KHz stereo
- 16-bit FM music synthesis audio

Figure 2-1 Serial Interface Block Diagram



3.0 Signal Definitions

Figure 3-1 Pin Diagram

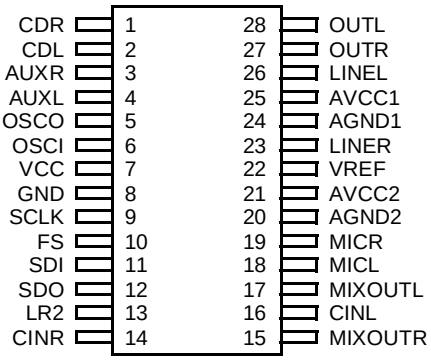


Table 3-1 Signal Descriptions

Signal Name	Pin No.	Pin Type	I/O Type	Signal Description
Serial Codec Interface Signals				
SCLK	9	O	TTL, 8mA bi-directional	***Serial Clock*** (Free running clock.)
SDI	11	I	TTL, Input	***Serial Data Input***
SDO	12	O	TTL, Output 8mA	***Serial Data Output***
LR2	13	I	TTL, Input	***DAC2 Sample Clock***
FS	10	I	TTL, Input	***Audio Codec Channel Select***
Codec/Mixer Interface Signals				
MICL, MICR	18, 19	I	Analog	***Microphone Inputs Left and Right***
LINEL, LINER	26, 23	I	Analog	***Line Inputs Left and Right***
CDL, CDR	2, 1	I	Analog	***CD Inputs Left and Right***
AUXL, AUXR	4, 3	I	Analog	***Auxiliary Inputs Left and Right***
OUTL, OUTR	28, 27	O	Analog (10kΩ, 25pF)	***Outputs Left and Right***
MIXOUTL, MIXOUTR	17, 15	O	Analog	***Mixer Outputs Left and Right***
CINL, CINR	16, 14	I	Analog	***ADC Filter Pins Left and Right***
VREF	22	I	Analog	***Voltage Reference***
OSCI	6	O	CMOS	***Oscillator Input***
OSCO	5	O	CMOS	***Oscillator Output***
Power and Ground Pins				
VCC	7	I	PWR	***Power Connection***
GND	8	I	GND	***Ground Connection***
AVCC2, AVCC1	21, 25	I	PWR	***Analog Power Connections***
AGND2, AGND1	20, 24	I	GND	***Analog Ground Connections***

4.0 Slot Assignment

The timing diagram in Figure 4-1 shows how the 82C916 assigns 16-bit time slots for various events via the SDI (Serial Data In) and SDO (Serial Data Out) pins. Table 4-1 summarizes how the SDI and SDO pins react during specific time slots followed with detailed bit information.

Figure 4-1 Timing Slot Assignment

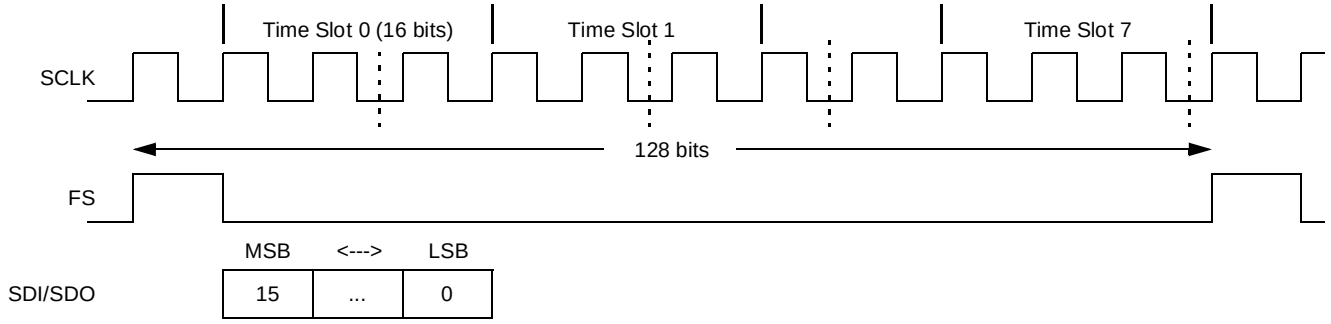


Table 4-1 Slot Assignment

Time Slot	SDI	SDO
0	Control Word Input	Status Word Output
1	Register Write Data	Register Read Data
2	DAC1 L	ADC L
3	DAC1 R	ADC R
4	DAC2 L	Reserved, set to 0
5	DAC2 R	Reserved, set to 0
6	Reserved	Reserved
7	Reserved	Reserved

Slot 0: Control / Status

SDI: Control Word Input

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved				DA2RV	DA2LV	DA1RV	DA1LV	R/nW	Reserved	IA[5:0]					
				DAC2 Right Channel Input Valid	DAC2 Left Channel Input Valid	DAC1 Right Channel Input Valid	DAC1 Left Channel Input Valid	Read/ not Write Request: 1 = Read		Index Address					

SDO: Status Word Output

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved						ADRV	ADLV	Reserved				DA2RRQ	DA2LRQ	DA1RRQ	DA1LRQ
						Right ADC Channel Output Valid	Left ADC Channel Output Valid					DAC2 Right Channel Input Request	DAC2 Left Channel Input Request	DAC1 Right Channel Input Request	DAC1 Left Channel Input Request

Note: Playback data is latched in the frame when both Channel Input Valid and Channel Input Request are TRUE.

Slot 1: Control Register Data

- SDI: Register Write Data
  - When a write is requested, data to be written must be transmitted in Slot 1 of the current frame, and the former contents of the Control Register are transmitted out during Slot 1 of the following frame.
- SDO: Register Read Data
  - The contents of the Control Register addressed is transmitted out during Slot 1 of the following frame.

Slot 2: Left Channel Playback and Capture Data 1

- SDI: DAC1 L
  - DAC1 Left Channel Playback Data. 16-bit, 2's complement PCM data, MSB first.
- SDO: ADC L
  - ADC Left Channel Capture Data. 16-bit, 2's complement PCM data, MSB first.

Slot 3: Right Channel Playback and Capture Data 1

- SDI: DAC1 Right
  - DAC1 Right Channel Playback Data. 16-bit, 2's complement PCM data, MSB first.
- SDO: ADC R
  - ADC Right Channel Capture Data. 16-bit, 2's complement PCM data, MSB first.

Slot 4: Left Channel Playback Data 2

- SDI: DAC2 Left
  - DAC2 Left Channel Playback Data. 16-bit, 2's complement PCM data, MSB first.
- SDO: Reserved, set to 0.

Slot 5: Right Channel Playback Data 2

- SDI: DAC2 Right
  - DAC1 Left Channel Playback Data. 16-bit, 2's complement PCM data, MSB first.
- SDO: Reserved, set to 0.

5.0 Register Descriptions

Table 5-1 shows a register map for the 82C916 (register-compatible with OPTi's 82C931). Table 5-2 gives detailed register bit information.

Table 5-1 82C916 Register Map

Index Address	Register Name	7	6	5	4	3	2	1	0
00h	MIXOUTL	LSS1	LSS0	LMGE	--	LAG3	LAG2	LAG1	LAG0
01h	MIXOUTR	RSS1	RSS0	RMGE	--	RAG3	RAG2	RAG1	RAG0
02h	CDL	LX1M	--	--	LX1G4	LX1G3	LX1G2	LX1G1	--
03h	CDR	RX1M	--	--	RX2G4	RX2G3	RX2G2	RX2G1	--
04h	FML	LFM	--	--	LX2G4	LX2G3	LX2G2	LX2G1	--
05h	FMR	RFM	--	--	RX1G4	RX1G3	RX1G2	RX1G1	--
06h	DACL	LDM	--	--	LDA4	LDA3	LDA2	LDA1	LDA0
07h	DACR	RDM	--	--	RDA4	RDA3	RDA2	RDA1	RDA0
08h-0Fh	Reserved								
10h	AUXL	LX2M	--	--	LX1G4	LX1G3	LX1G2	LX1G1	--
11h	AUXR	RX2M	--	--	RX1G4	RX1G3	RX1G2	RX1G1	--
12h	LINEL	LLM	--	--	LLG4	LLG3	LLG2	LLG1	--
13h	LINER	RLM	--	--	RLG4	RLG3	RLG2	RLG1	--
14h	MICL	LMM	RMME	--	LMG4	LMG3	LMG2	LMG1	--
15h	MICR	RMM	LMME	--	RMG4	RMG3	RMG2	RMG1	--
16h	OUTL	LOM	ZCEN	LOG5	LOG4	LOG3	LOG2	LOG1	--
17h	OUTR	ROM	--	ROG5	ROG4	ROG3	ROG2	ROG1	--
18h-1Fh	Reserved								

Note: "--" indicates reserved bits - must be written to 0.

Table 5-2 82C916 Register/Bit Formats

7	6	5	4	3	2	1	0
Index Address 00h			**MIXOUT Left Output Control Register**				
LSS1	LSS0	LMGE	--	LAG3	LAG2	LAG1	LAG0
Source select: 00 = LINE 10 = MIC 01 = CD 11 = MIXER		MIC +20dB Gain: 0 = Disable 1 = Enable	Reserved	Gain select for MIXOUTL (dB): 0000 = 0 0110 = +9.0 1011 = +16.5 0001 = +1.5 0111 = +10.5 1100 = +18.0 0010 = +3.0 1000 = +12.0 1101 = +19.5 0011 = +4.5 1001 = +13.5 1110 = +21.0 0100 = +6.0 1010 = +15.0 1111 = +22.5 0101 = +7.5			
Index Address 01h			**MIXOUT Right Output Control Register**				
RSS1	RSS0	RMGE	--	RAG3	RAG2	RAG1	RAG0
Source select: 00 = LINE 10 = MIC 01 = CD 11 = MIXER		MIC +20dB Gain: 0 = Disable 1 = Enable	Reserved	Gain select for MIXOUTR (dB): Refer to 00h[3:0] for decode.			
Index Address 02h			**CD Left Input Control Register**				
LX1M	--	--	LX1G4	LX1G3	LX1G2	LX1G1	--
Mute: 0 = Disable 1 = Enable	Reserved		Gain select for CDL (dB): 0000 = +12 0110 = –6 1011 = –21 0001 = +9 0111 = –9 1100 = –24 0010 = +6 1000 = –12 1101 = –27 0011 = +3 1001 = –15 1110 = –30 0100 = 0 1010 = –18 1111 = –33 0101 = –3 Note: This decode is also applicable for the MIC, LINE, AUX, and FM inputs.				Reserved
Index Address 03h			**CD Right Input Control Register**				
RX1M	--	--	RX2G4	RX2G3	RX2G2	RX2G1	--
Mute: 0 = Disable 1 = Enable	Reserved		Gain select CDR (dB): Refer to 02h[4:1] for decode.				Reserved
Index Address 04h			**FM Left Input Control Register**				
LFM	--	--	LX2G4	LX2G3	LX2G2	LX2G1	--
Mute: 0 = Disable 1 = Enable	Reserved		Gain select FML (dB): Refer to 02h[4:1] for decode.				Reserved

Table 5-2 82C916 Register/Bit Formats (cont.)

7	6	5	4	3	2	1	0
Index Address 05h			**FM Right Input Control Register**				
RFM	--	--	RX1G4	RX1G3	RX1G2	RX1G1	--
Mute: 0 = Disable 1 = Enable	Reserved		Gain select FMR (dB): Refer to 02h[4:1] for decode.				Reserved
Index Address 06h			**DAC Left Input Control Register**				
LDM	--	--	LDA4	LDA3	LDA2	LDA1	LDA0
Mute: 0 = Disable 1 = Enable	Reserved		Gain select for DAC inputs (dB): *00000 = 0 00001 = –1.5 00010 = –3.0 00011 = –4.5 00100 = –6.0 00101 = –7.5 00110 = –9.0 00111 = –10.5	01000 = –12.0 01001 = –13.5 01010 = –15.0 01011 = –16.5 01100 = –18.0 01101 = –19.5 01110 = –21.0 01111 = –22.5	10000 = –24.0 10001 = –25.5 10010 = –27.0 10011 = –28.5 10100 = –30.0 10101 = –31.5 10110 = –33.0 10111 = –34.5		11000 = –36.0 11001 = –37.5 11010 = –39.0 11011 = –40.5 11100 = –42.0 11101 = –43.5 11110 = –45.0 11111 = –46.5
Index Address 07h			**DAC Right Input Control Register**				
RDM	--	--	RDA4	RDA3	RDA2	RDA1	RDA0
Mute: 0 = Disable 1 = Enable	Reserved		Gain select for DAC inputs (dB): Refer to 06h[4:0] for decode.				
Index Address 08h-0Fh			**Reserved**				
Index Address 10h			**AUX Left Input Control Register**				
LX2M	--	--	LX1G4	LX1G3	LX1G2	LX1G1	--
Mute: 0 = Disable 1 = Enable	Reserved		Gain select for AUXL (dB): Refer to 02h[4:1] for decode.				Reserved
Index Address 11h			**AUX Right Input Control Register**				
RX2M	--	--	RX1G4	RX1G3	RX1G2	RX1G1	--
Mute: 0 = Disable 1 = Enable	Reserved		Gain select for AUXR (dB): Refer to 02h[4:1] for decode.				Reserved
Index Address 12h			**LINE Left Input Control Register**				
LLM	--	--	LLG4	LLG3	LLG2	LLG1	--
Mute: 0 = Disable 1 = Enable	Reserved		Gain select for LINEL (dB): Refer to 02h[4:1] for decode.				Reserved

Table 5-2 82C916 Register/Bit Formats (cont.)

7	6	5	4	3	2	1	0
Index Address 13h			**LINE Right Input Control Register**				
RLM	--	--	RLG4	RLG3	RLG2	RLG1	--
Mute: 0 = Disable 1 = Enable	Reserved		Gain select for LINER inputs (dB): Refer to 02h[4:1] for decode.				Reserved
Index Address 14h			**MIC Left Input Control Register**				
LMM	RMME	--	LMG4	LMG3	LMG2	LMG1	--
Mute: 0 = Disable 1 = Enable	MICR mixed into OUTL: 0 = Disable 1 = Enable	Reserved	Gain select for MICL (dB): Refer to 02h[4:1] for decode.				Reserved
Index Address 15h			**MIC Right Input Control Register**				
LMM	RMME	--	LMG4	LMG3	LMG2	LMG1	--
Mute: 0 = Disable 1 = Enable	MICL mixed into OUTR: 0 = Disable 1 = Enable	Reserved	Gain select for MICR (dB): Refer to 02h[4:1] for decode.				Reserved
Index Address 16h			**OUT Left Output Control Register**				
LOM	ZCEN	LOG5	LOG4	LOG3	LOG2	LOG1	--
Mute: 0 = Disable 1 = Enable	Reserved	Gain select for OUTL (dB): 00000 = 0 00001 = –3 00010 = –6 00011 = –9 00100 = –12 00101 = –15 00110 = –18 00111 = –21	 01000 = –24 01001 = –27 01010 = –30 01011 = –33 01100 = –36 01101 = –39 01110 = –42 01111 = –45	 10000 = –48 10001 = –51 10010 = –54 10011 = –57 10100 = –60 10101 = –63 10110 = –66 10111 = –69	 11000 = –72 11001 = –75 11010 = –78 11011 = –81 11100 = –84 11101 = –87 11110 = –90 11111 = –93		Reserved
Index Address 17h			**OUT Right Output Control Register**				
LOM	--	LOG5	LOG4	LOG3	LOG2	LOG1	--
Mute: 0 = Disable 1 = Enable	Reserved	Gain select for OUTR (dB): Refer to 16h[5:1] for decode.					Reserved
Index Address 18h-1Fh			**Reserved**				

6.0 Electrical Specifications

Stresses above those listed in the following tables may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification are not implied.

6.1 Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit
VCC	Supply Voltage	4.5	5.5	V
AVCC	Analog Supply Voltage	4.75	5.25	V
VIN	Input Voltage	–0.5	VCC + 0.5	V
VOUT	Output Voltage	–0.5	VCC + 0.5	V
TOP	Operating Temperature	0	70	°C
TSTG	Storage Temperature	–40	125	°C
ESD[a]	ESD Tolerance (Human Body Model MIL883C, 3015.7, Notice 8)		1000	V

a. ESD senstive device. Electrostatic charges as high as 4000V readily accumulate on the human body and test equipment and can discharge without detection. Although the 82C931 features ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

6.2 DC Characteristics: 5.0 Volt (VCC = 5.0V ±5%, TA = 0°C to +70°C)

Symbol	Parameter	Min	Max	Unit	Condition
VIL	Low Level Input Voltage	–0.3	0.8	V	VCC = 5.5V
VIH	High Level Input Voltage	2.4	VCC + 0.3	V	VCC = 4.5V
VIHa	High Level Input Voltage for RESET	3.5	VCC + 0.3	V	VCC = 4.5V
VOL	Low Level Output Voltage		0.2	V	IOL = 4mA, VCC = 4.5
VOH	High Level Output Voltage	VCC – 0.5	5.5	V	IOH = –4mA VCC = 5.5V
IIL	Input Leakage Current		10	µA	VCC = 5.5V
IILa	Input Leakage Current with 5K ohm Pull-up Resistor	–100	–500	µA	VIN = 0V
IILb	Input Leakage Current with 50K ohm Pull-up Resistor	–10	–50	µA	VIN = 0V
IOL	Output Leakage Current		10	µA	VCC = 5.5V
IPD	Static or Power-down Mode Current		300	µA	VCC = 5.5V

6.3 General Specifications: 5.0 Volt (VCC = 5.0V ±5%, TA = 0°C to +70°C)

Symbol	Parameter	Min	Typ	Max	Unit	Condition
IIL	Low Level Input Current	–10		10	µA	VIN = GND
IIH	High Level Input Current	–10		10	µA	VIN = VCC
IOZ	Tristate Output Leakage Current	–10		10	µA	VOUT = 0/VCC
V-	Schmitt Negative Threshold	0.8 1.5		1.3 2.5	V	TTL-STATIC CMOS-STATIC
V+	Schmitt Positive Threshold	1.4 2.5		2.1 3.5	V	TTL-STATIC CMOS-STATIC
VH	Schmitt Hysteresis		0.6 1.0		V	TTL-STATIC CMOS-STATIC
VIL	low Level Input Voltage			0.8	V	TTL-STATIC
VIH	High Level Input Voltage	2.0			V	TTL-STATIC
VOL	Low Level Output Voltage			0.4	V	TTL-STATIC
VOH	High Level Output Voltage	2.4			V	TTL-STATIC
RPD	Pull-down Resistance	50		200	KΩ	VIN = VCC
RPU	Pull-up Resistance	50		200	KΩ	VIN = VCC
CIN	Input Capacitance			5	pF	Frequency = 1MHz @ 0V
COUT	Output Capacitance			5	pF	Frequency = 1MHz @ 0V
CIO	Bidirectional Capacitance			5	pF	Frequency = 1MHz @ 0V
IOS	Short Circuit Output Current		2	25	mA	VOUT = 0V
IKLU	I/O Latch-Up Current	100			mA	V < GND, V > VCC
VESD	Electrostatic Protection	2000			V	C = 100pF, R = 1.5KΩ

6.4 Pin Specifications - Analog (VCC = 5.0V, 25°C)

Pin Name	Parameter	Min	Typ	Max	Unit	Condition
Inputs						
MICR, MICL, LINER, LINEL, CDR, CDL, AUXR, AUXL, CINR, CINL	Signal Bandwidth Input Range (AC)	10 0.0		20K 2.0	Hz V	Sine Wave
Outputs						
OUTR, OUTL	Signal Bandwidth Output Range	10 0.85		20K 2.85	Hz V	Sine Wave Load = 10KΩ, 25pF
MIXOUTR, MIXOUTL	Signal Bandwidth Output Range	10 0.85		20K 2.85	Hz	Sine Wave
VREF			1.85		V	DC

6.5 Volume Setting

Parameter	Min	Typ	Max	Unit	Test Conditions
Input Gain/Atten. Range: 16 levels (MIC, LINE, CD, AUX) 16 levels (ADC) 32 levels (DAC) 32 levels (LOUT)	 –33 0 –93 –46.5		 12 22.5 0 0	dB	Input @ 1Hz, 2.5Vpp wrt ACOM
Step Size: 16 levels (MIC, LINE, CD, AUX) 16 levels (ADC) 32 levels (DAC) 32 levels (LOUT)	 2.6 1.3 2.6 2.0 1.3	 3.0 1.5 3.0 3.0 1.5	 3.4 1.7 3.4 4.0 1.7	dB	 90 to -81dB) (-84 to -93dB)
Mute Level		–80		dB	
Signal to Noise Ratio		–80		dB	
Total Harmonic Distortion		0.04		%	
Total Dynamic Range		80		dB	
Interchannel Isolation		60		dB	
Interchannel Gain Mismatch	–0.5		0.5	dB	
Gain Drift		100		ppm/°C	

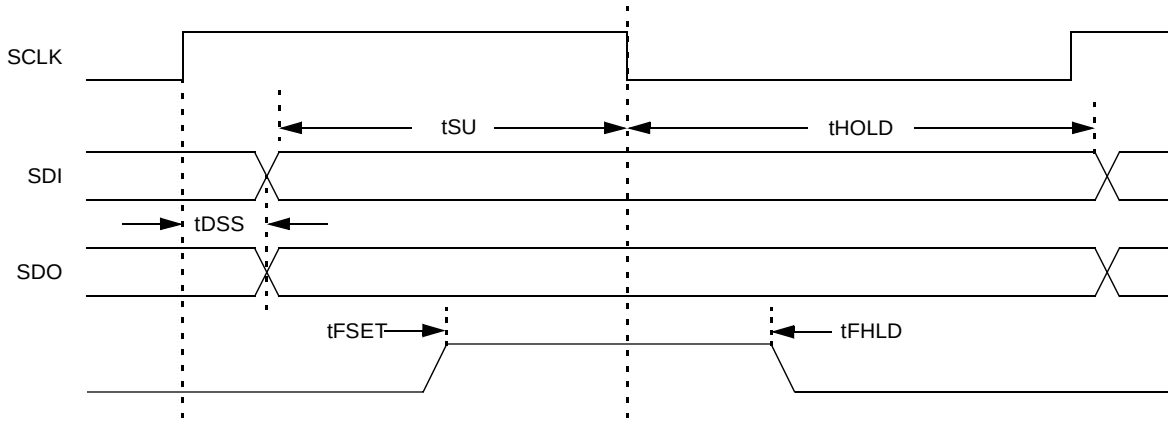
6.6 ADC/DAC Converters

Parameter	Min	Typ	Max	Unit	Test Conditions
Analog-to-Digital Converter					
Resolution		16		Bits	
SNR (Signal-to-Noise Reduction)	75	82		dB	
DC Offset			±10	mV	
Digital-to-Analog Converter					
Full-scale output voltage	2			Vpp	
Resolution		16		Bits	
SNR (Signal-to-Noise Reduction)	75	82		dB	

6.7 AC Timings

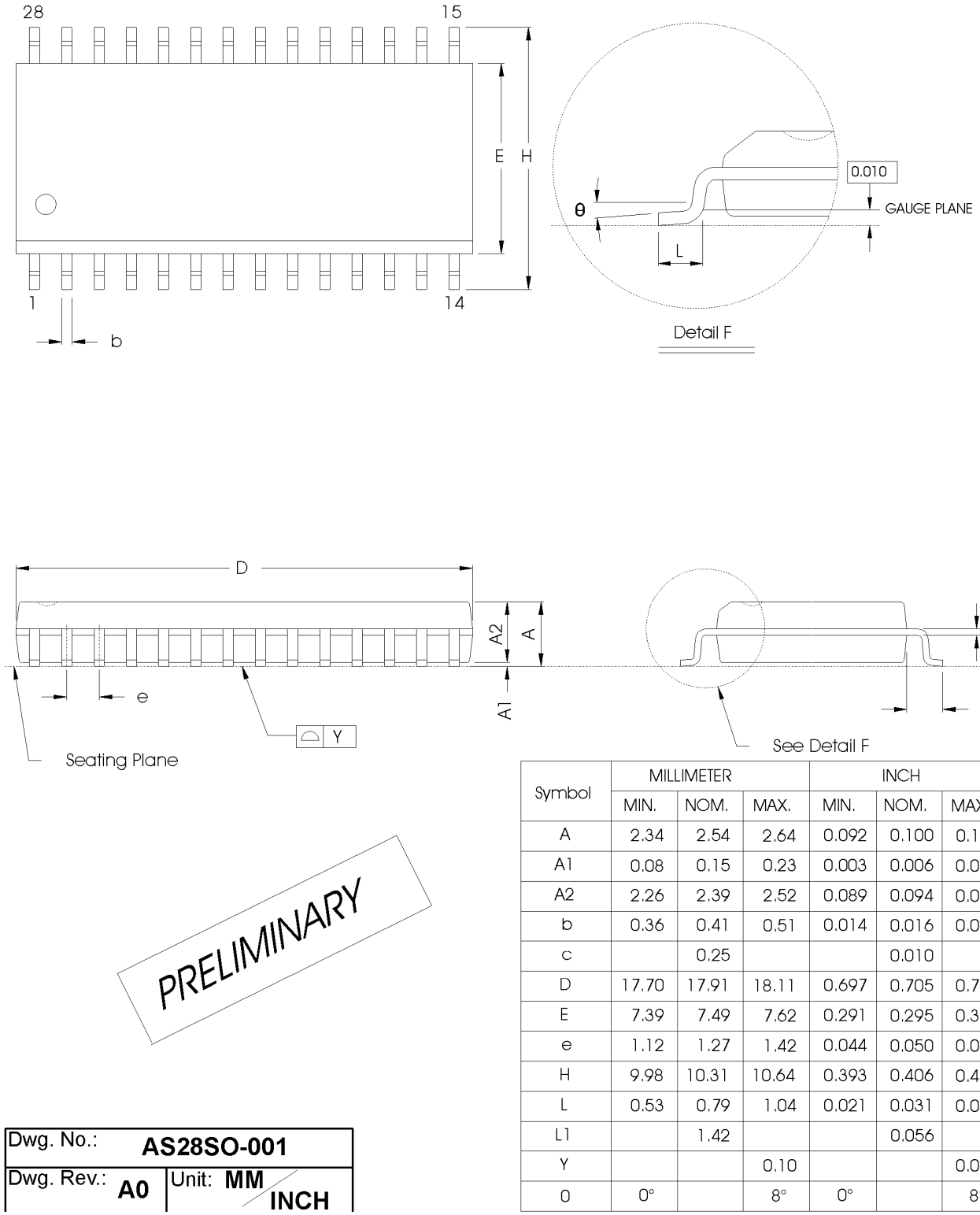
Symbol	Parameter	Min	Max	Unit	Condition
tSU	SDI to SCLK Setup	10		ns	Vcc=5V, 25°C
tHOLD	SCLK to SDI Hold	10		ns	
tFHLD	Seek to FS Hold	10		ns	
tDSS	SCLK Positive Edge to SDO		15	ns	
tFSET	FS to SLCK Setup	10		ns	

Figure 6-1 Host Serial Interface Timing Waveform



7.0 Mechanical Package Outline

Figure 7-1 28-pin Small Outline Package (SOP, 300mm)



Symbol	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	2.34	2.54	2.64	0.092	0.100	0.104
A1	0.08	0.15	0.23	0.003	0.006	0.009
A2	2.26	2.39	2.52	0.089	0.094	0.099
b	0.36	0.41	0.51	0.014	0.016	0.020
c		0.25			0.010	
D	17.70	17.91	18.11	0.697	0.705	0.713
E	7.39	7.49	7.62	0.291	0.295	0.300
e	1.12	1.27	1.42	0.044	0.050	0.056
H	9.98	10.31	10.64	0.393	0.406	0.419
L	0.53	0.79	1.04	0.021	0.031	0.041
L1		1.42			0.056	
Y			0.10			0.004
θ	0°		8°	0°		8°

PRELIMINARY

Dwg. No.:	AS28SO-001		
Dwg. Rev.:	A0	Unit:	MM / INCH

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