

ConnectCore for i.MX6UL Single Board Computer

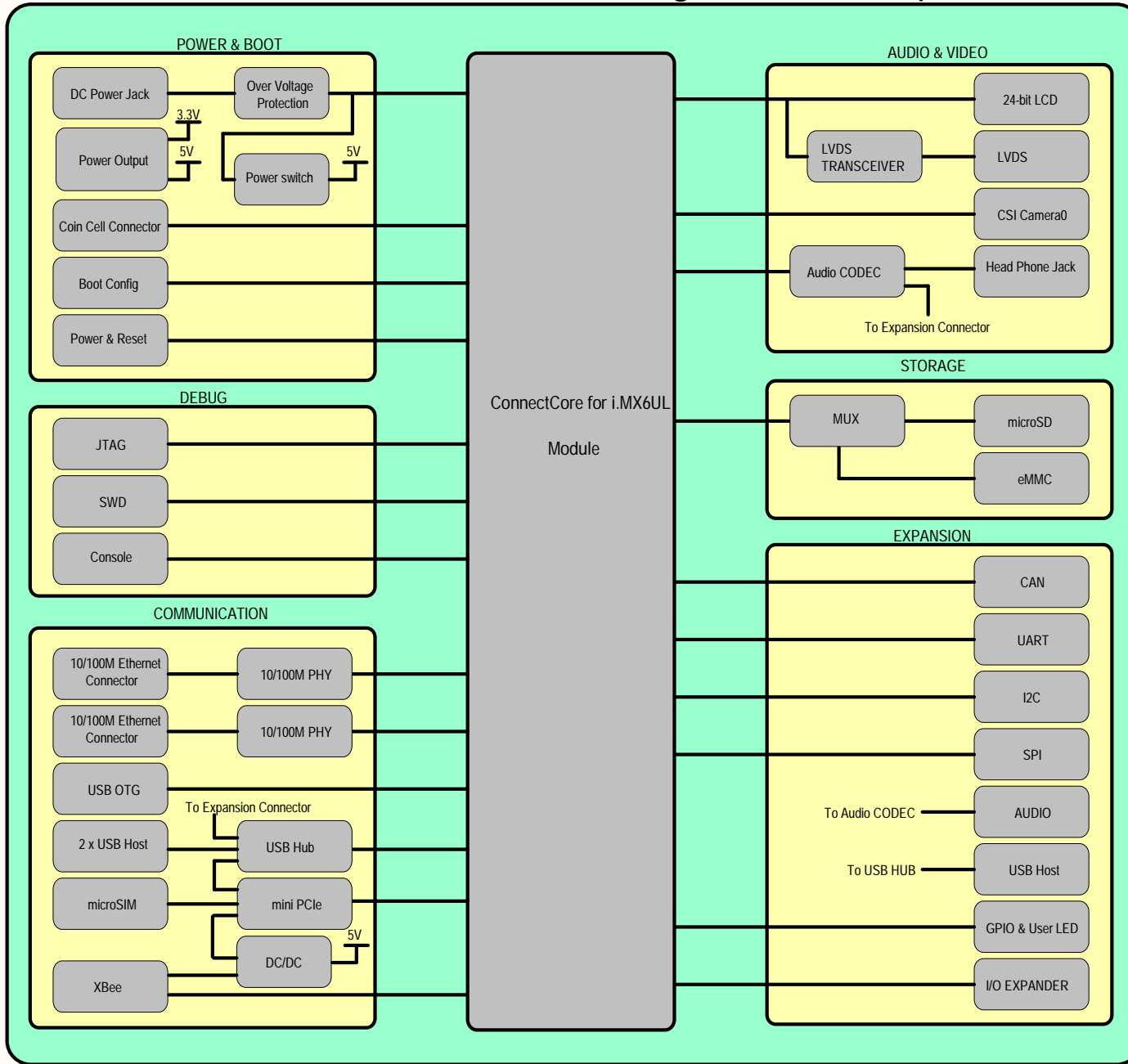
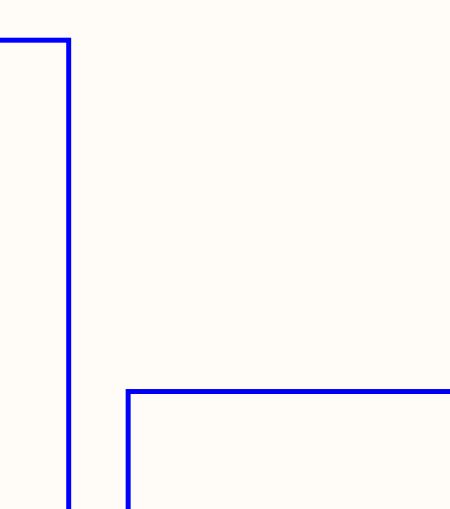
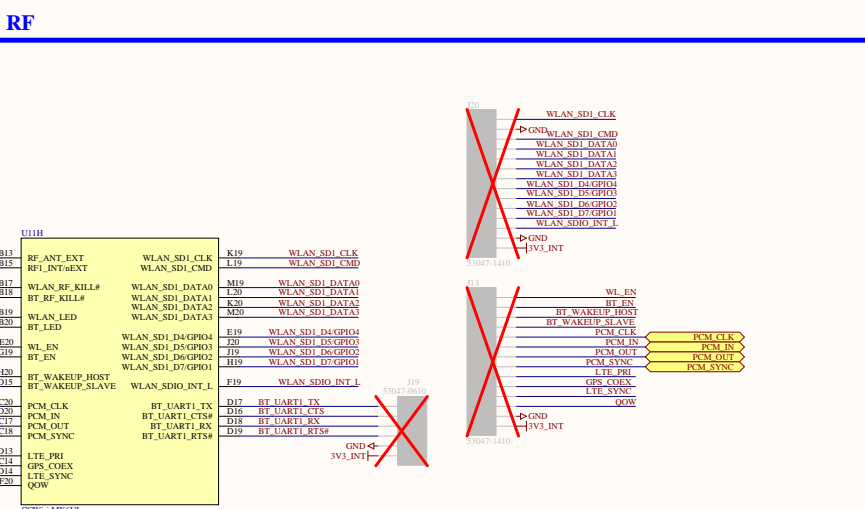
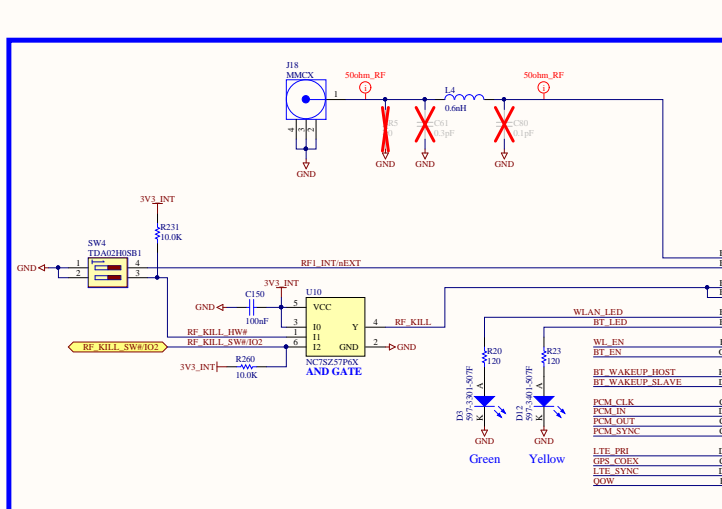
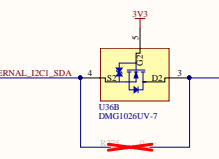
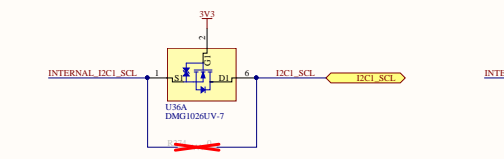
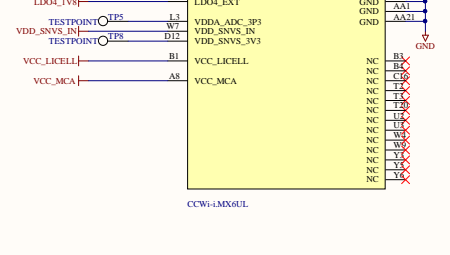
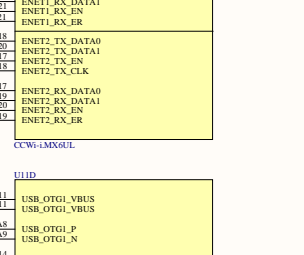
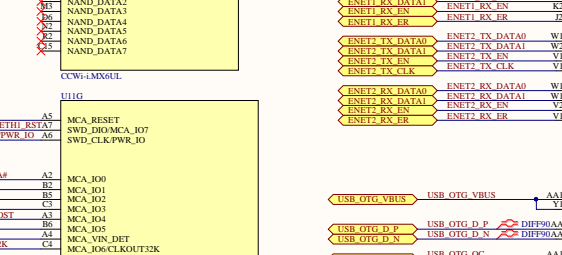
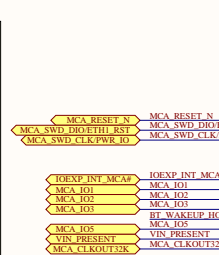
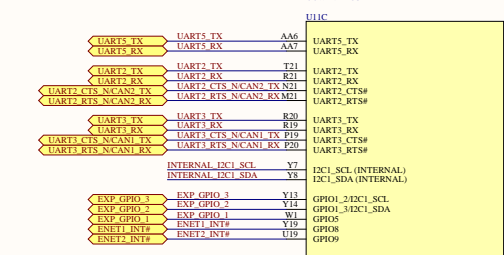
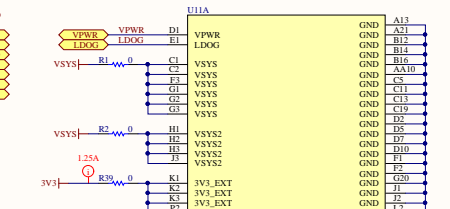
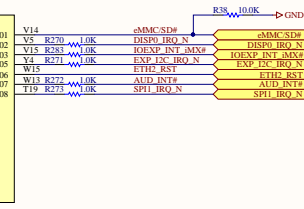
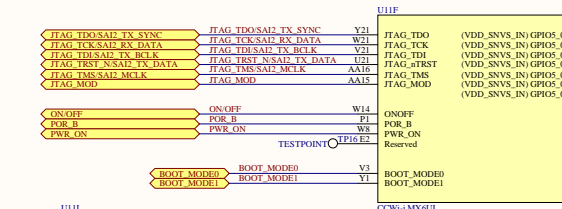
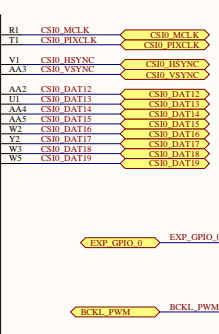
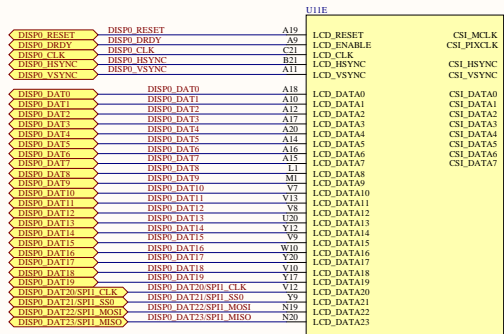


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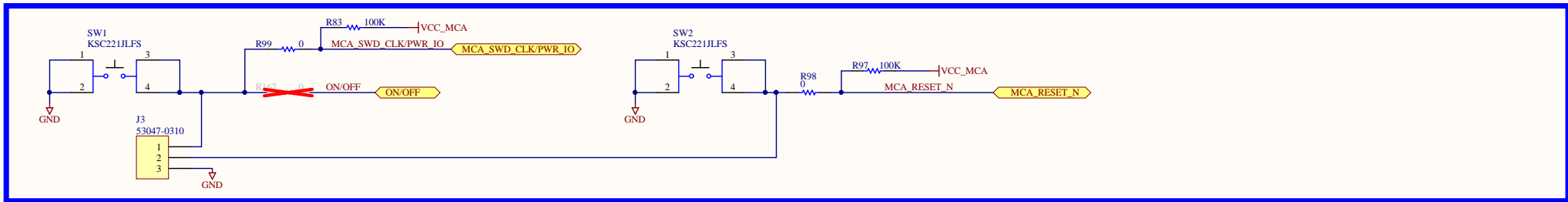
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ConnectCore for i.MX6UL Module



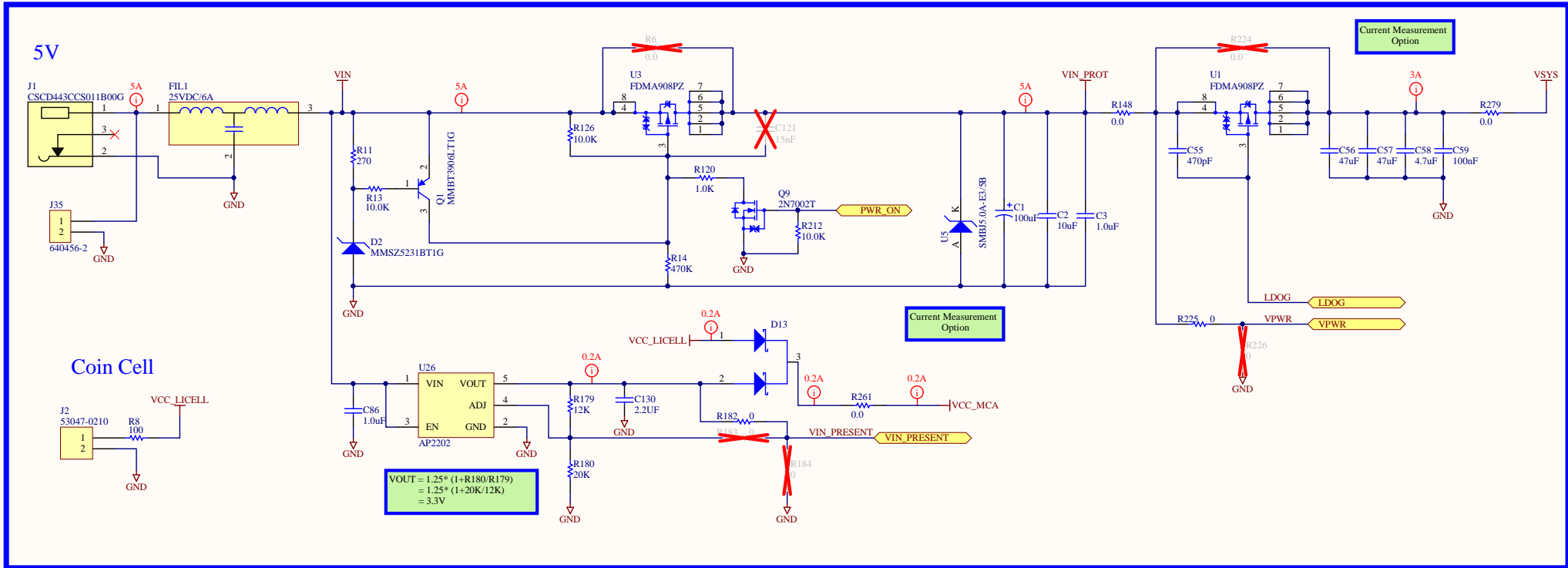
PRELIMINARY

Power and Reset



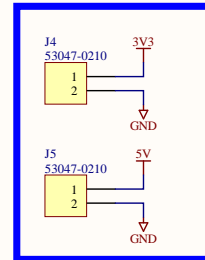
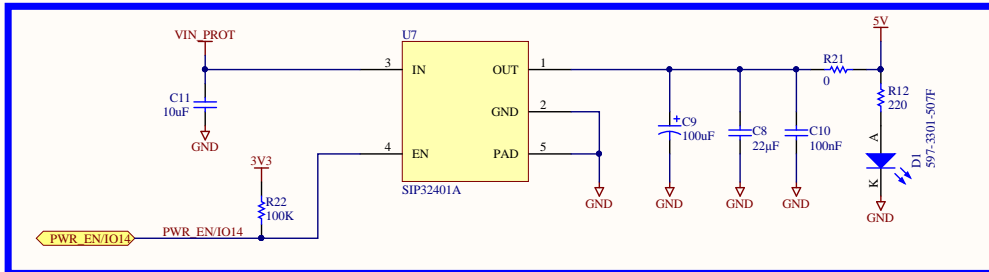
Supply Inputs

Over Voltage Protection

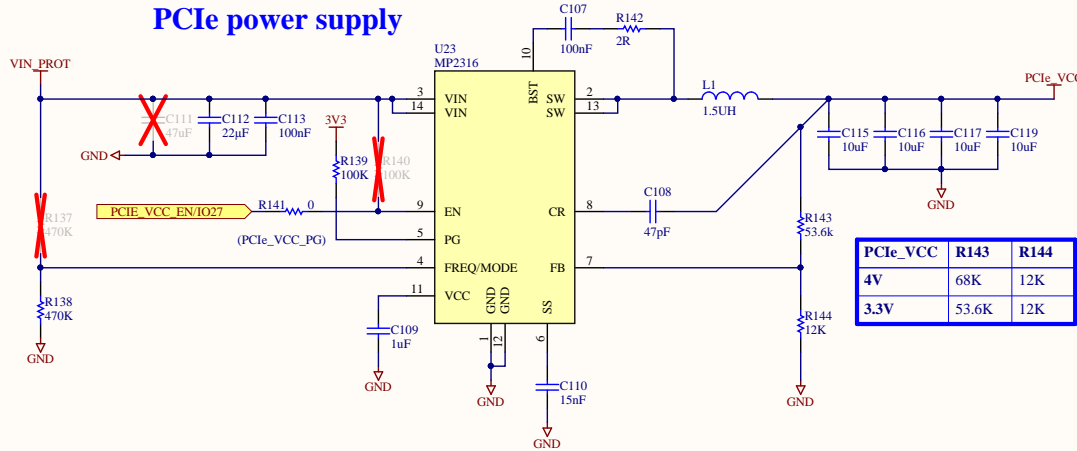


5V Load switch

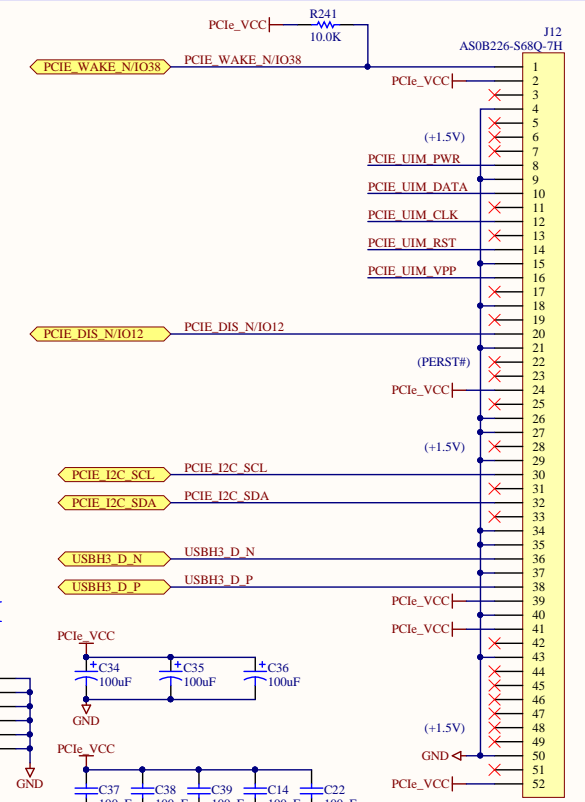
Supply Outputs



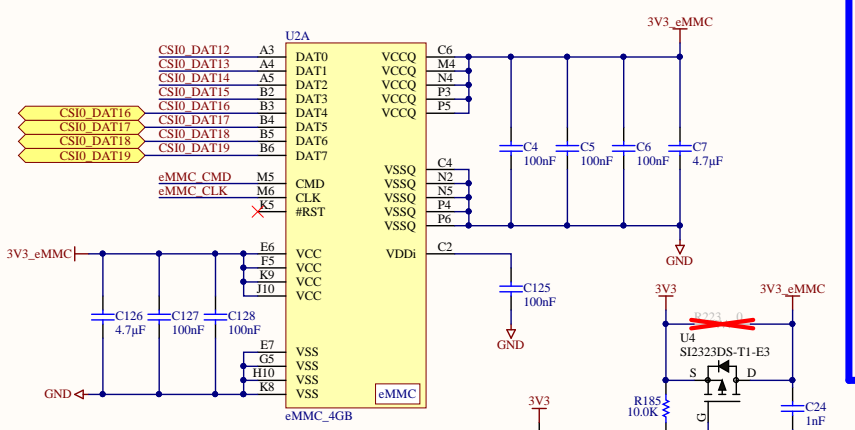
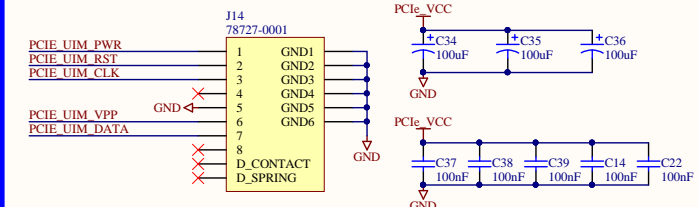
PCIe power supply



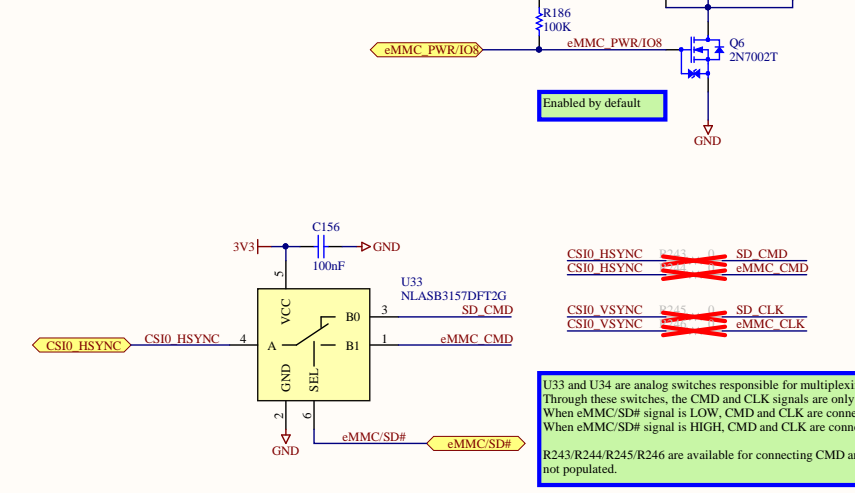
miniPCIe



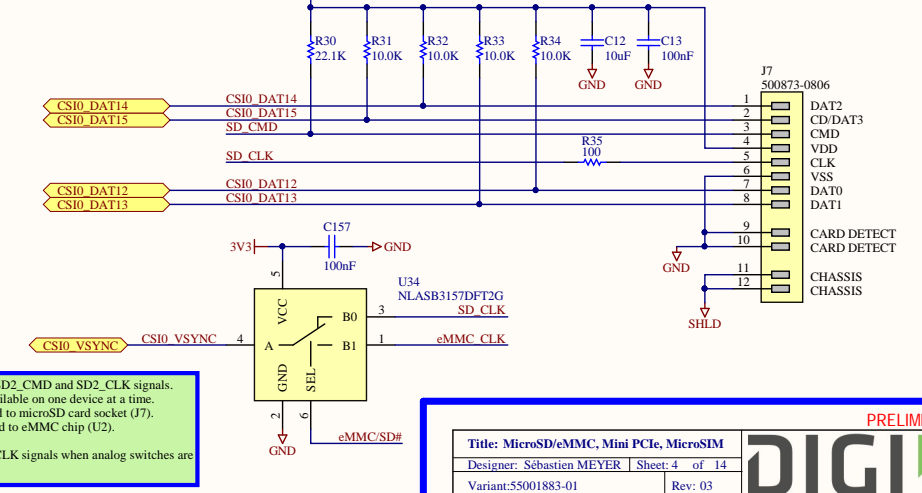
micro SIM



eMMC



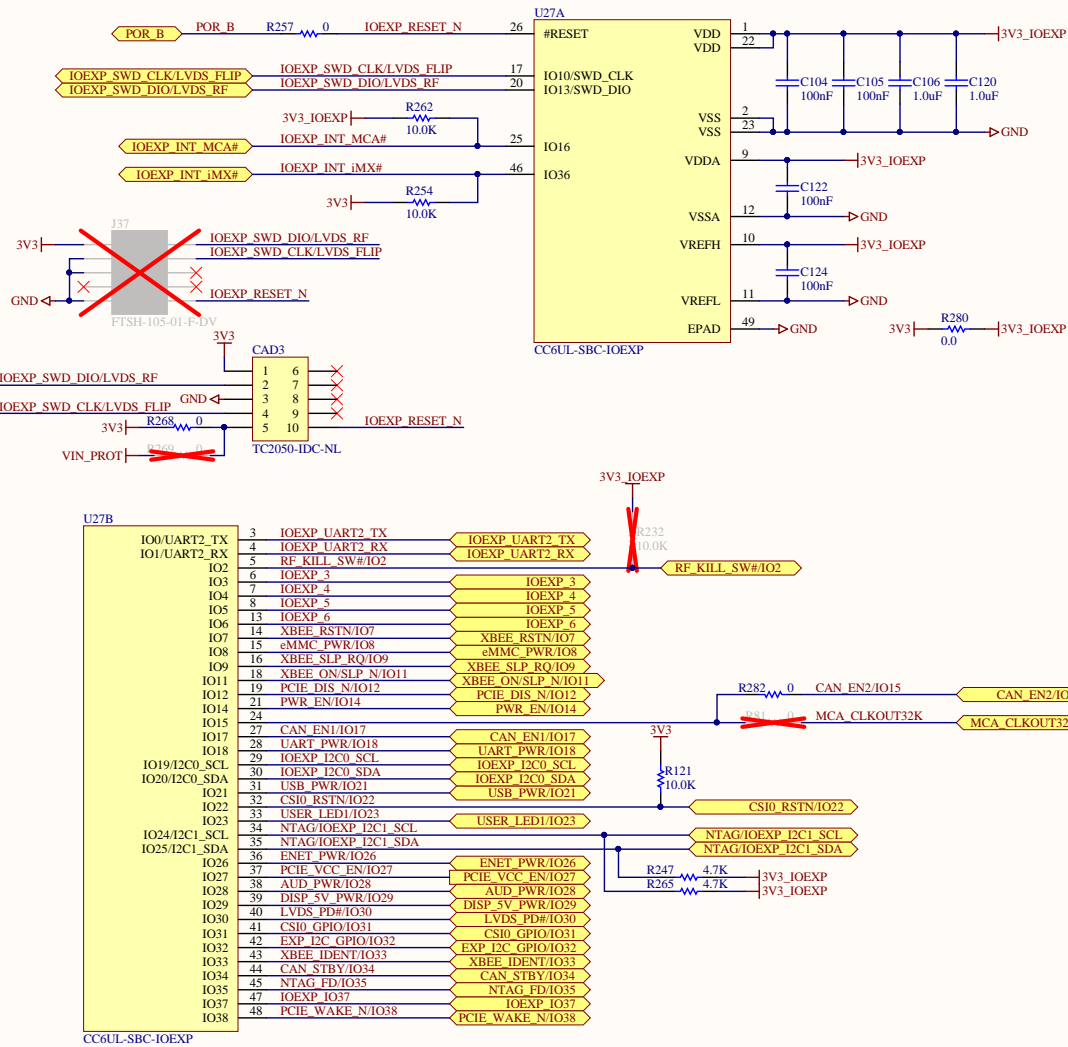
microSD



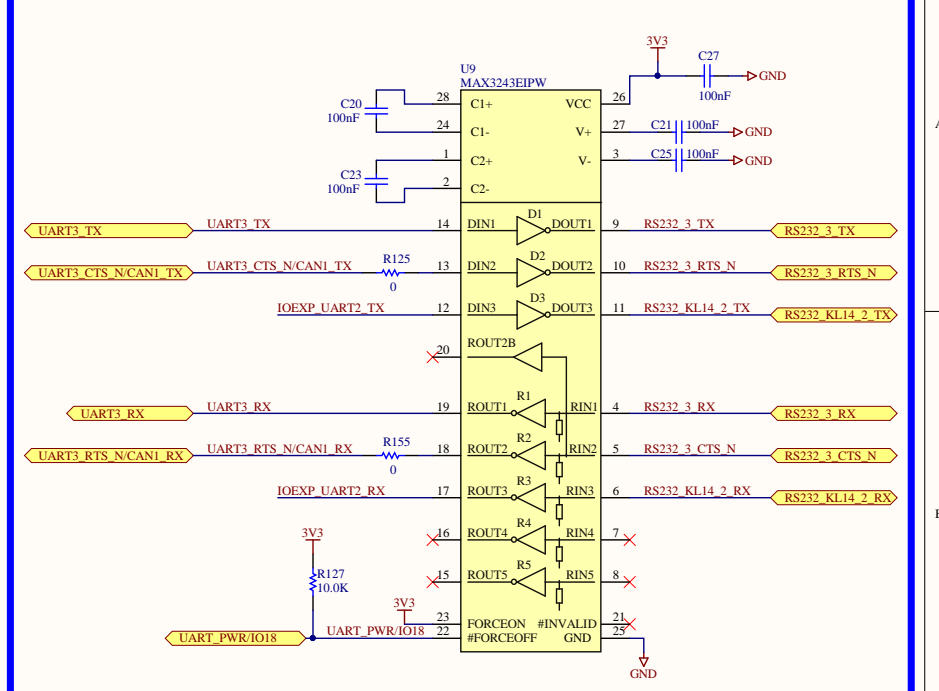
U33 and U34 are analog switches responsible for multiplexing SD2_CMD and SD2_CLK signals. Through these switches, the CMD and CLK signals are only available on one device at a time. When eMMC/SD# signal is LOW, CMD and CLK are connected to microSD card socket (J7). When eMMC/SD# signal is HIGH, CMD and CLK are connected to eMMC chip (U2).

R243/R244/R245/R246 are available for connecting CMD and CLK signals when analog switches are not populated.

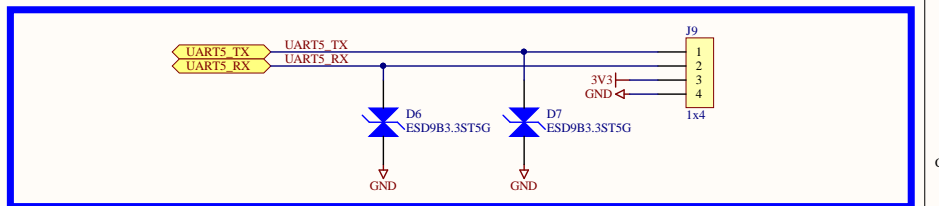
I/O EXPANDER



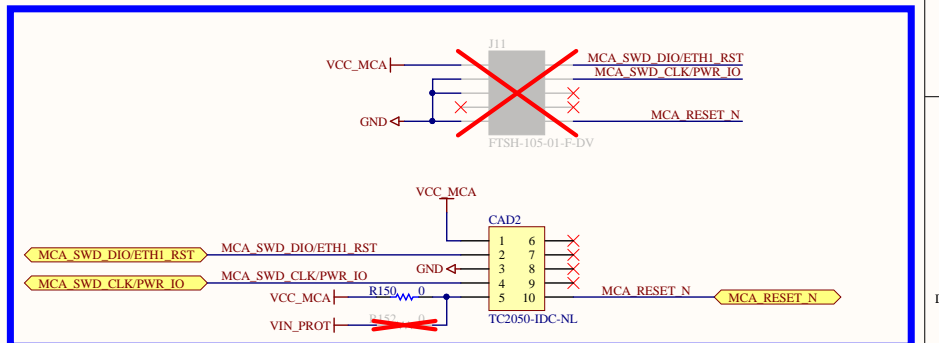
UART 1&3



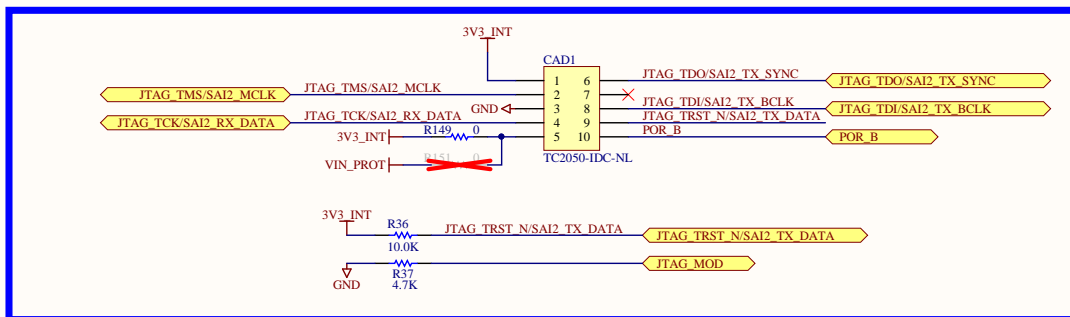
Console TTL



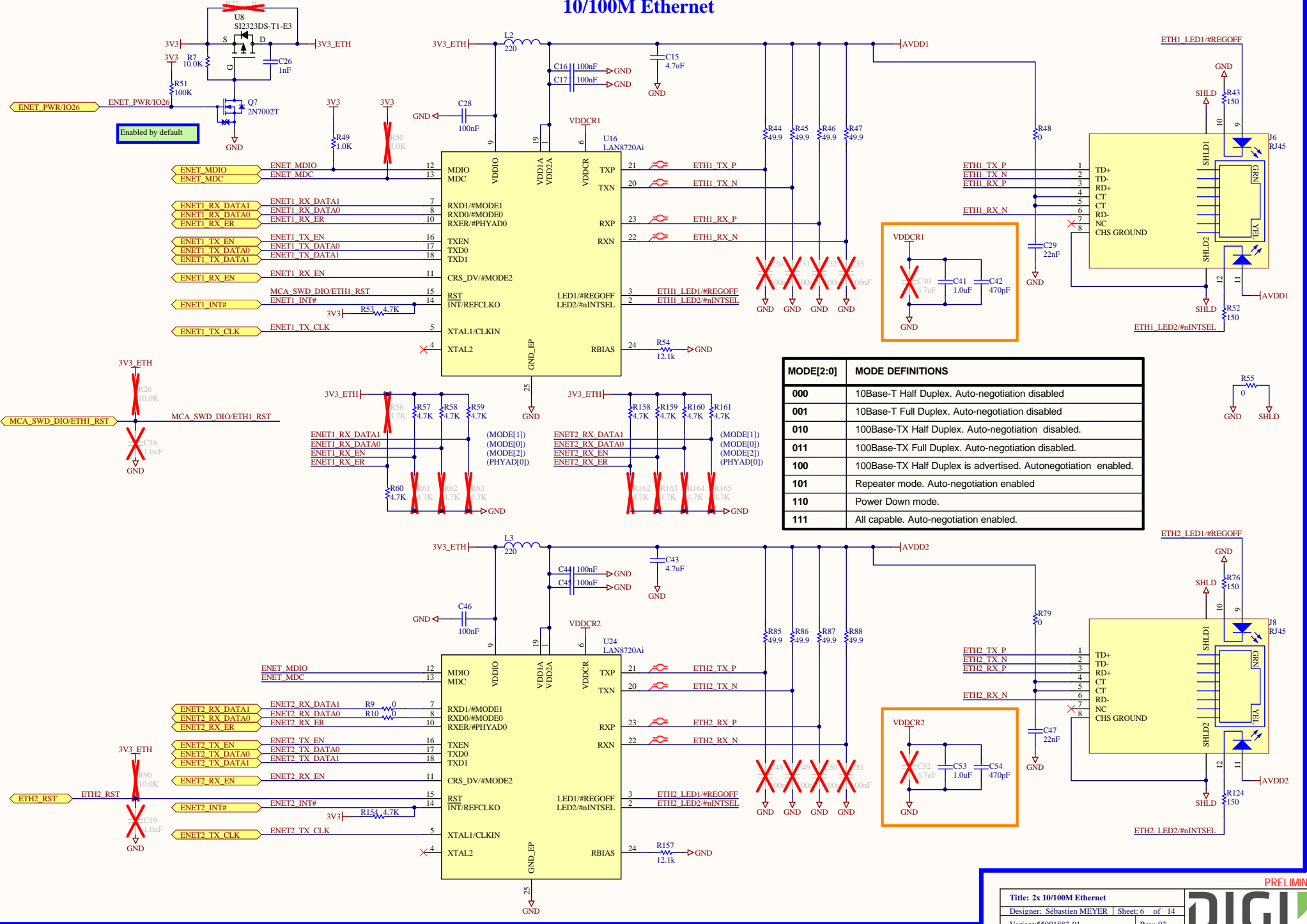
SWD



JTAG

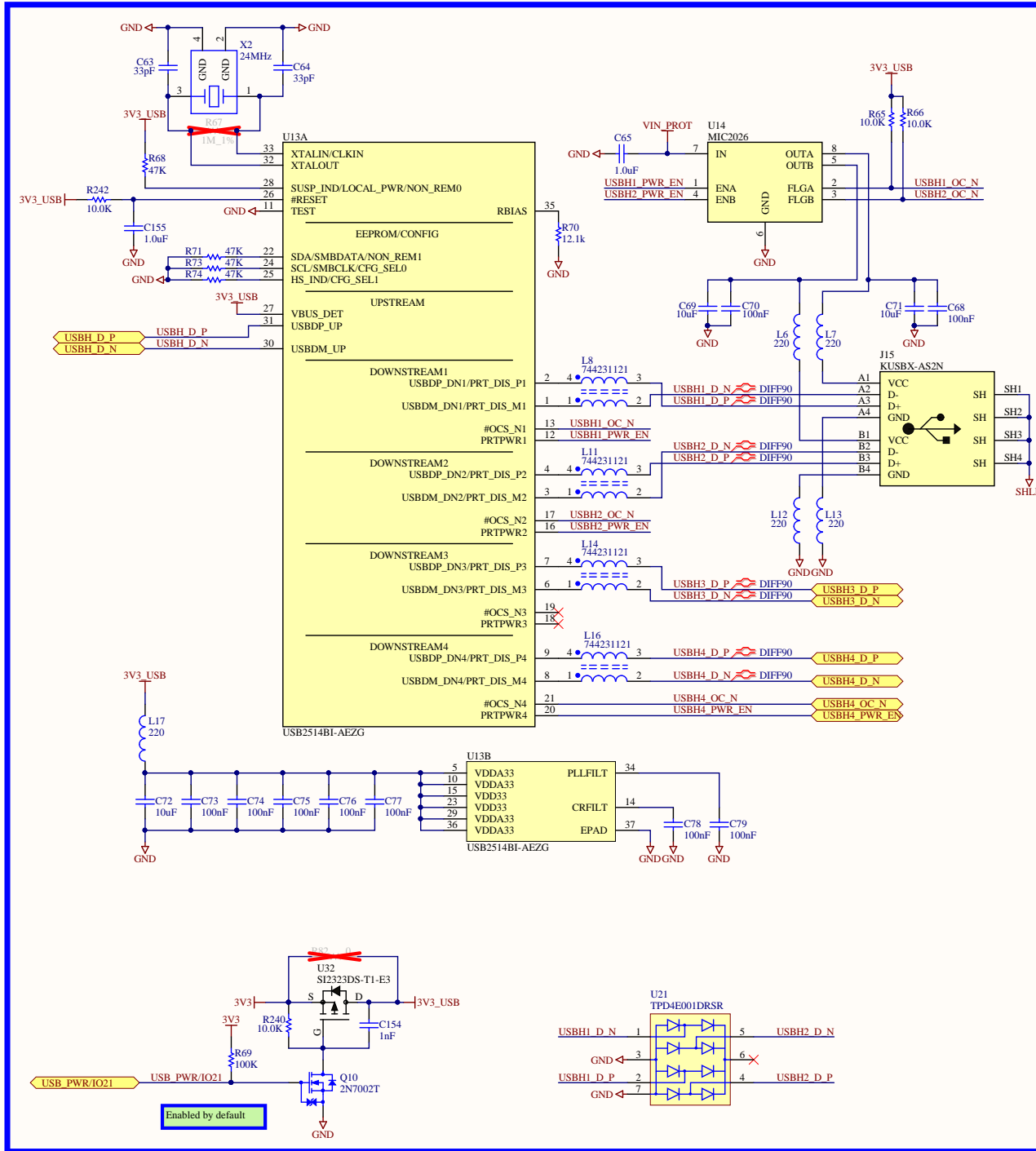


10/100M Ethernet

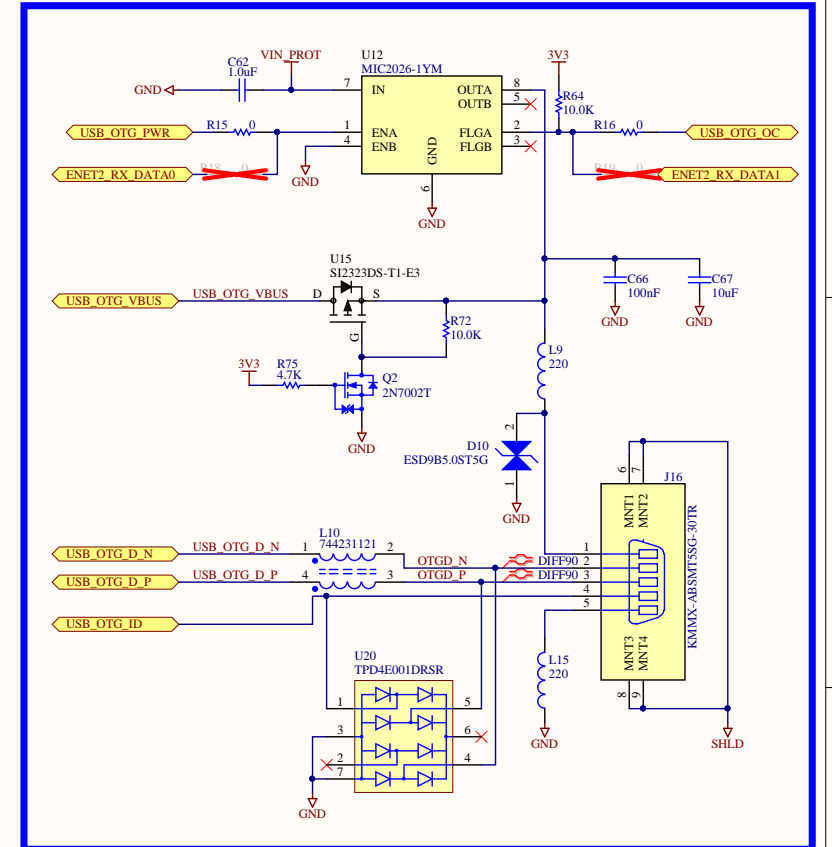


MODE[2:0]	MODE DEFINITIONS
000	10Base-T Half Duplex. Auto-negotiation disabled
001	10Base-T Full Duplex. Auto-negotiation disabled
010	100Base-TX Half Duplex. Auto-negotiation disabled.
011	100Base-TX Full Duplex. Auto-negotiation disabled.
100	100Base-TX Half Duplex is advertised. Autonegotiation enabled.
101	Repeater mode. Auto-negotiation enabled
110	Power Down mode.
111	All capable. Auto-negotiation enabled.

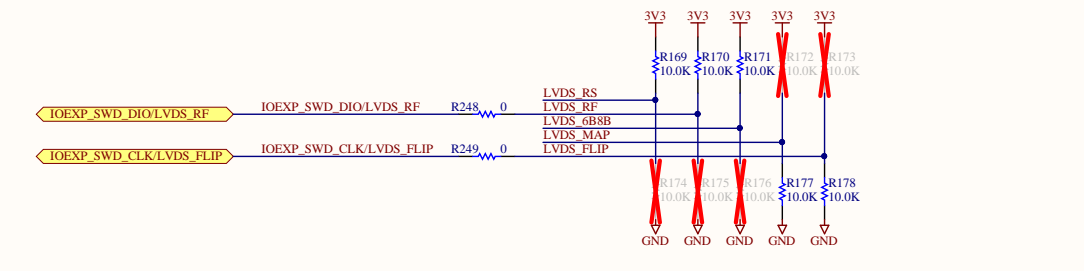
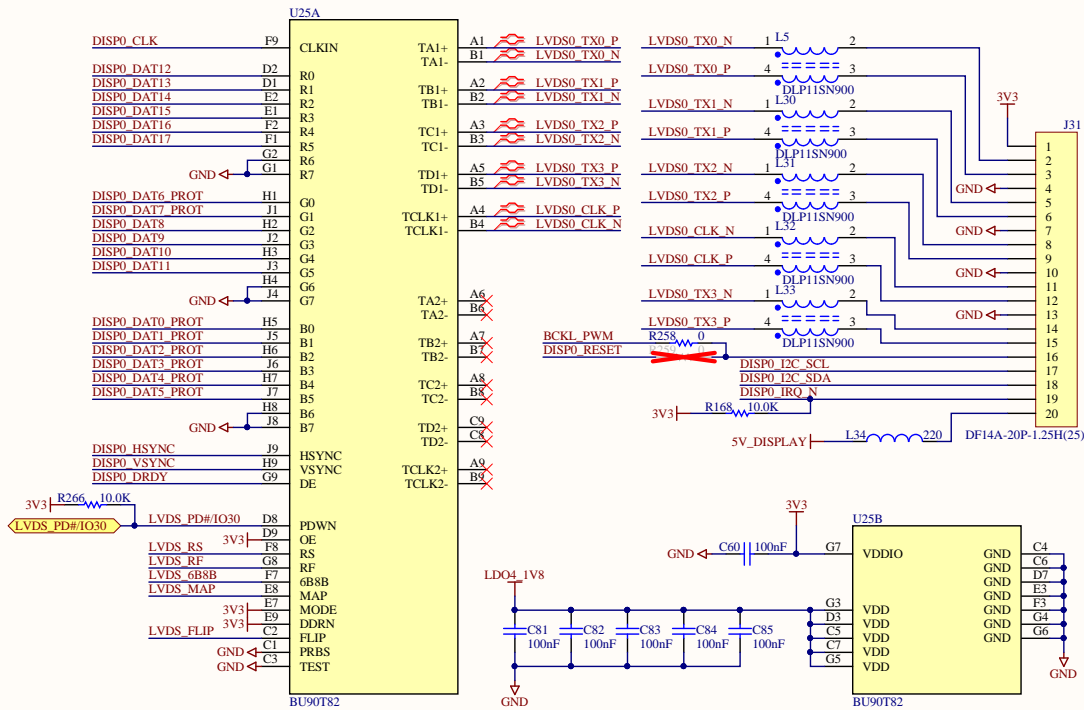
USB_HOST



USB_OTG



LVDS



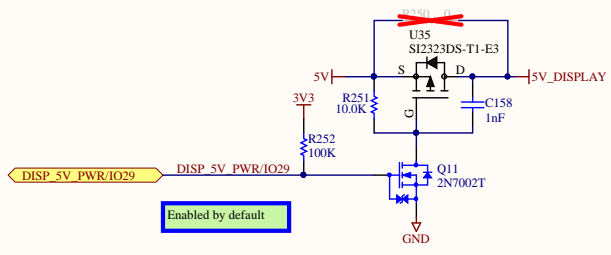
LVDS_RS: LVDS Swing Mode Select:
 H: 350mV
 L: 200mV

LVDS_RF: Input CLK Triggering Edge Select:
 H: Rising Edge
 L: Falling Edge

LVDS_6B8B: 6bit/8bit Mode Select:
 H: 6bit mode (TD1+/-, TD2+/- outputs are Hi-Z)
 L: 8bit mode

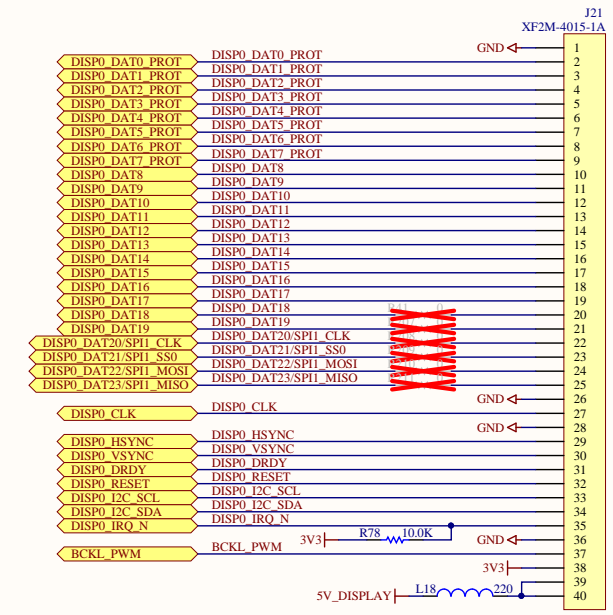
LVDS_MAP: LVDS Output Data Mapping Select:
 H: JEIDA
 L: VESA

LVDS_FLIP: LVDS Output Pin Reverse Select:
 H: Reverse
 L: Normal



Enabled by default

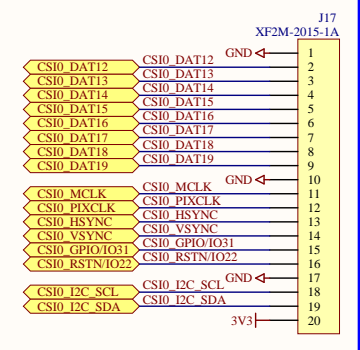
Parallel Display 0



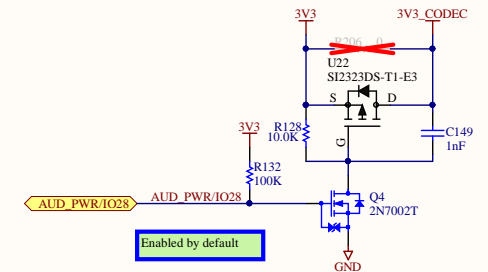
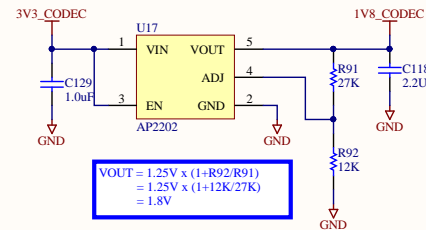
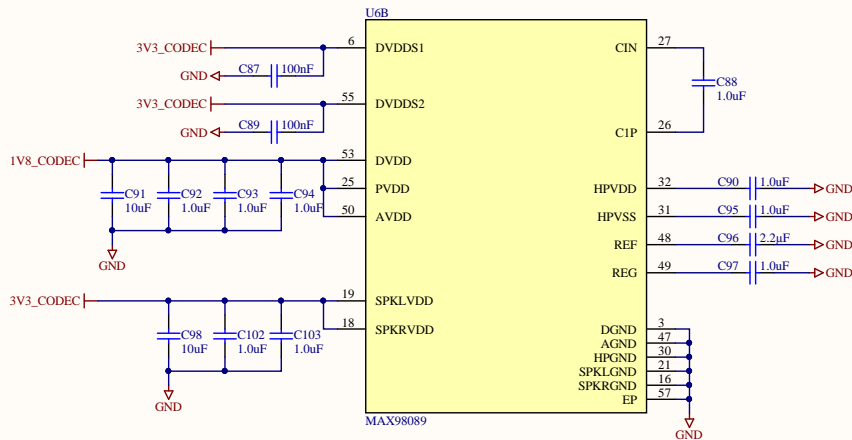
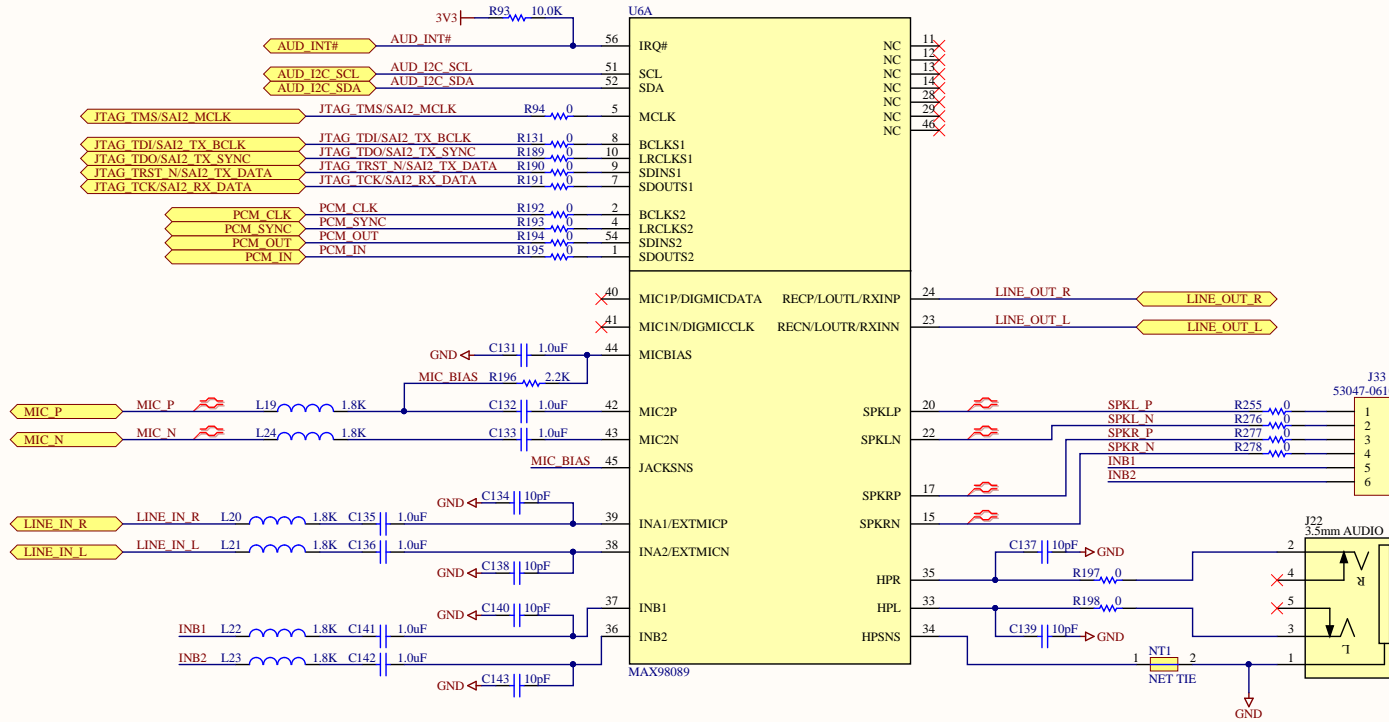
3V3 maximum current allowed on J21: 0.5A
 5V maximum current allowed on J21: 1A

If higher currents are required on boards connected to J21, an external supply must be used to power them.

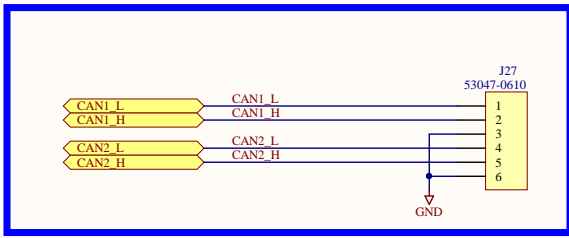
Parallel Camera 0



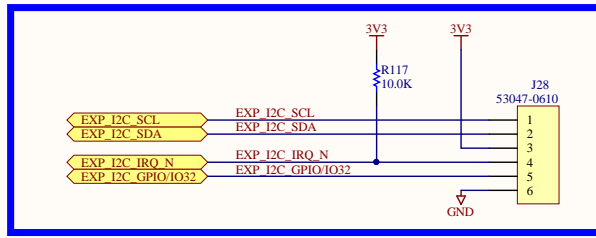
AUDIO



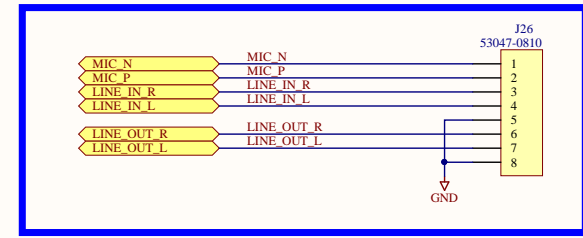
CAN



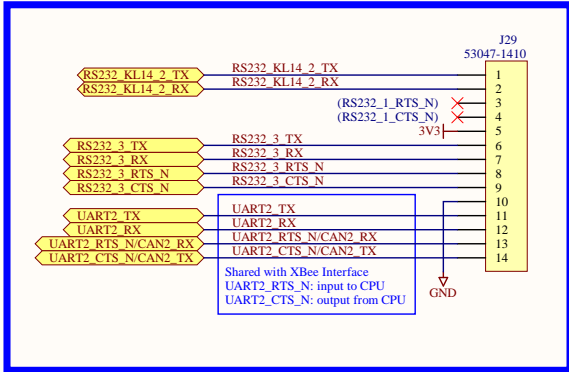
I2C



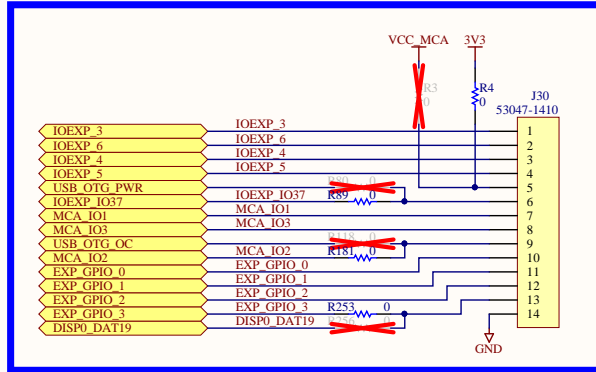
AUDIO



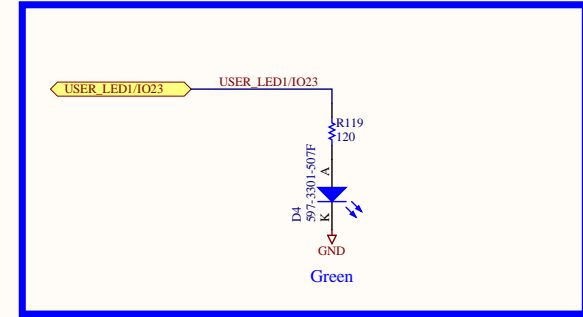
UART



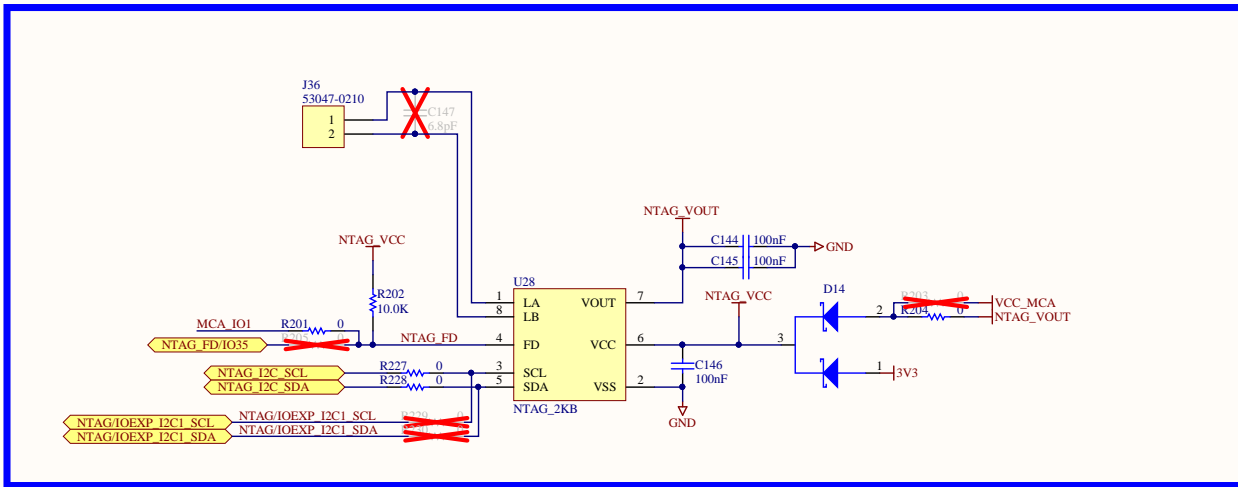
GPIO



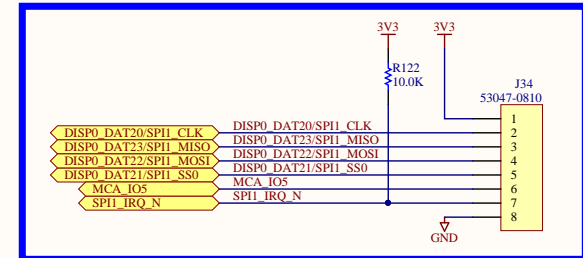
USER LED



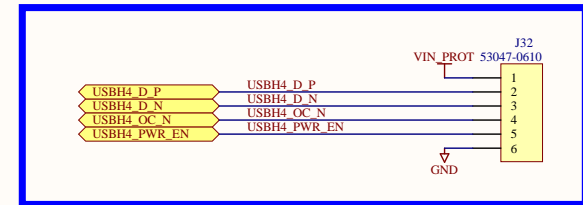
NFC NTAG I2C



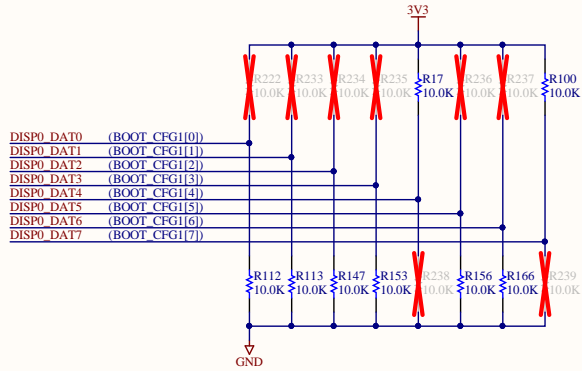
SPI



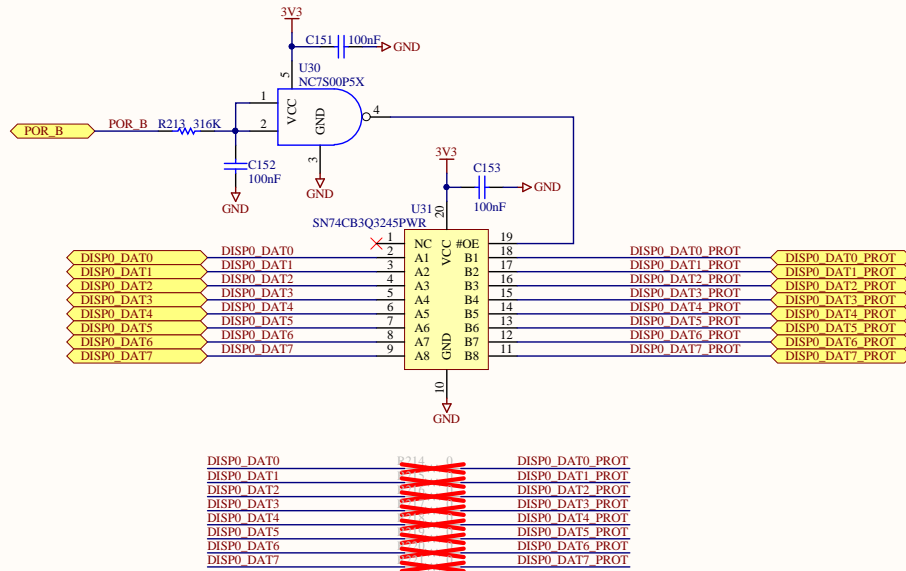
USB



Bootstrap

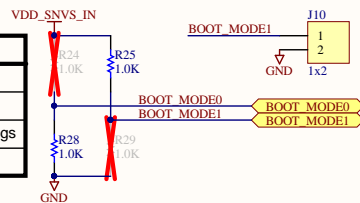


BOOTSTRAP	NAND
BOOT_CFG1[0]	Row Address Cycles: 00 - 3 cycles 01 - 2 cycles 10 - 4 cycles 11 - 5 cycles
BOOT_CFG1[1]	
BOOT_CFG1[2]	Number of devices: 00 - 1 device 01 - 2 devices 10 - 4 devices 11 - Reserved
BOOT_CFG1[3]	
BOOT_CFG1[4]	Pages in Block: 00 - 128 pages 01 - 64 pages 10 - 32 pages 11 - 256 pages
BOOT_CFG1[5]	
BOOT_CFG1[6]	Samsung's toggle mode DDR NAND 0 - Raw NAND 1 - Toggle mode NAND
BOOT_CFG1[7]	Boot Device Selection: 1 - Boot from NAND interface



Boot Mode

BOOT_MODE1	BOOT_MODE0	Description
0	0	Boot from Fuses
0	1	Serial Downloader
1	0	Boot from board settings
1	1	Reserved



System Power Rails

Voltage (V)	Supply Name	Block	Generated by	Current Capability (mA)	Notes
5.0	VIN	Overvoltage Prot	External DC supply	-	
		MCA LDO			
	VIN_PROT	ConnectCore 6UL	Overvoltage Prot	-	
		5V load switch			
		USB Host VBUS			
		USB OTG VBUS			
	5V	LVDS0	Load switch (U7)	-	
		Parallel LCD			
		CC6UL VBUS			
3.3	3V3	eMMC	PMIC SW2	1250	
		microSD			
		UART RS-232			
		KL14 (I/O EXP)			
		2x10/100M ENET			
		USB Hub			
		LVDS			
		Parallel LCD			
		Parallel Camera			
		AUDIO			
		CAN1/2			
	XBee				
	NTAG				
	PCIe_VCC	PCIe minicard	VIN_PROT	3000	
	VCC_MCA	MCA	AP2202	150	
3.0	VCC_LICELL	RTC	External Coin Cell	-	
	VDD_SNV5_IN	BOOT	PMIC VSNVS	-	
1.8	LDO4_1V8	LVDS	PMIC LDO4	350	
	1V8_CODEC	AUDIO	AP2202	150	

GPIO Table

Signal Name	GPIO	Use
i.MX6UL processor		
GPIO1_5	GPIO1_5	EXP_GPIO_1
GPIO1_8	GPIO1_8	ENET1_INT#
GPIO1_9	GPIO1_9	ENET2_INT#
NAND_CE1#	GPIO4_14	EXP_GPIO_0
GPIO5_01	GPIO5_01	eMMC/SD#
GPIO5_02	GPIO5_02	DISP0_IRQ_N
GPIO5_03	GPIO5_03	IOEXP_INT_iMX#
GPIO5_05	GPIO5_05	EXP_I2C_IRQ_N
GPIO5_06	GPIO5_06	ETH2_RST
GPIO5_07	GPIO5_07	AUD_INT#
GPIO5_08	GPIO5_08	SPI1_IRQ_N
MCA (KL03)		
SWD_CLK	PTA0	PWR_IO
MCA_IO0	PTB0/LLWU_P4	KL4_INT_MCA#
MCA_IO4	PTA9	BT_WAKEUP_HOST

Format: DD/MM/YYYY

12/02/2016 - ConnectCore i.MX6UL Single Board Computer

* Initial version

19/09/2016 - ConnectCore i.MX6UL module

* Revision: 03 - NPR004795

- PCB spin: 3001517x-01 revA => 3001517x-02 revA

