# UNC20 Module

User's Manual


P.O: Box 1103
Kueferstrasse 8
Tel. +49 (7667) 908-0
sales@fsforth.de

- D-79200 Breisach, Germany
- D-79206 Breisach, Germany
- Fax +49 (7667) 908-200
- http://www.fsforth.de

FS Forth-Systeme GmbH
Postfach 1103, 79200 Breisach, Germany

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Author: N. James
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## Table of Contents

## 1. General

The Universal Network Controller (UNC20) has been designed for embedded systems requiring network connectivity. The UNC20 module is housed in an industry-standard DIL48 package, making it extremely easy and cost-effective to integrate into designs which require Ethernet connectivity.

This document refers to the UNC20 modules with the Part Numbers 352 and 355.

## 2. Features

- NetSilicon's NS7520 microcontroller
- Up to 16Mbytes SDRAM, 32-bit wide
- Up to 8Mbytes Flash memory, 16-bit wide
- PHY for 10/100 Ethernet
- Two serial interfaces
- Serial EEPROM (8KBytes) for storing configuration parameters
- I2C port
- Up to 16 programmable digital I/O pins (multiplexed with other functions)
- JTAG interface
- External 8-bit data bus, 10-bit address bus and 2 external chip selects
- Single power supply of +3.3V required

# 3. Detailed Description

## 3.1. NS7520 Processor

The CPU is an ARM7TDMI 32-bit RISC core running at 55MHz with a rich complement of peripherals on-chip.

For more information on this device please consult the NS7520_HR.pdf document.

The ARM7TDMI is capable of operating in both little-endian and big-endian modes. The standard UNC20 modules, currently Part Numbers 352 and 355, are factory-configured to boot in big-endian mode.

## 3.2. Memory

The UNC20 is assembled with 16Mbytes of 32-bit wide SDRAM. A 16-bit wide Flash device is assembled. Currently 2 variants of the UNC20 are available, one with 2MB Flash (P/N 355) and one with 8MB Flash (P/N 352).

## 3.3. Ethernet Interface

The NS7520 contains a 10/100 Ethernet MAC which is conform to the IEEE802.3 standard. Included on-chip are a 512-byte transmit FIFO and 2-Kbyte receive FIFO for maximizing Ethernet throughput. Full-duplex and half-duplex modes are supported for both 10Mbps and 100 Mbps operations as is address filtering for broadcasts and multicasts.

The PHY on the module supports auto-negotiation and can drive a 100Base-Tx line or a 10Base-T line. The UNC20 provides 4 pins for connecting a Twisted-Pair RJ-45 interface using an external transformer with a 1:1 turns ratio.

## 3.4. Timers

Two independent 27-bit timers are provided in the NS7520. These can be programmed to generate interrupts after expiration of time periods ranging from 2us to 20 hrs. Both timers can be programmed to generate an interrupt to the ARM core on either the IRQ or FIQ signals.

## 3.5. General purpose I/O

Two 8-bit ports (A and C) are available for digital I/O. All pins are multi-function and can be individually configured. Pins C2 and C6 are reserved for the I2C bus. The other 14 pins can be freely configured by the user and may be used to implement a serial interface, for example. Pins C0, C1 and C3 can be used to generate a level-sensitive interrupt to the ARM core's IRQ signal.

## 3.6. Serial Interface

Two independent serial channels are available in the NS7520. These channels can operate in the following modes:

UART at speeds up to 230 kbits/sec, with 5 to 8 data bits; odd, even or no parity; 1 or 2 stop bits.

HDLC at speeds up to 4 Mbps

SPI (Serial Peripheral Interface) - this full-duplex synchronous 4-wire interface can be used to connect various peripherals to the UNC20.

The pins for the 2 serial channels are multiplexed with the 16 General Purpose I/O pins. Serial channel 1 is on Port C and the following signals are available: RxD, TxD, RTS, CTS, DCD, RI. Only 6 signals are available since 2 pins are used by the I2C interface. Serial channel 2 is on Port A and the same signals are available plus DSR and DTR. All signals are 3.3V TTL levels.

## 3.7. I2C

An I2C bus is available on pins 17 (SDA) and 21 (SCL). Any 3.3V I2C device can be connected to these pins provided that they do not use address 0xA0 which is being used by an 8-kByte EEPROM on the UNC20. The I2C bus can operate at speeds of 100 kbit/sec (Standard mode).

## 3.8. JTAG interface

This interface is primarily used for debug purposes. The 5 pins TCK, TMS, TDI, TDO and TRST# are multiplexed with 5 address lines and are available on pins 2 through 6. Selection of the JTAG signals is achieved by tying pin 30 (LEDLNK/SEL#) low. When pin 30 is not tied to GND it is the LEDLNK output from the PHY and is used to drive an LED on the base board to denote Ethernet link and activity.

## 3.9. Reset

A power-on reset generator resets all components on the module. The RESET# signal is output on pin 25 so that it can be used to reset components on the base board at power-on. The RESET# signal is bi-directional thus allowing devices on the base board, such as a reset switch, to reset the module. The RESET# signal can sink 5mA and source 150uA. These values must not be exceeded.

## 3.10. External peripheral bus

An 8-bit data bus and 10-bit address bus are provided for connecting external peripherals to the UNC20. Two individually programmable chip selects and an OE# (Output Enable) and WE# (Write Enable) signal allow a vast range of 8-bit peripherals to be connected directly to the UNC20 without any glue logic.

## 3.11. Voltage Requirements

For the UNC20 module only a single 3.3V DC power supply is needed.

## 4. UNC20 Connector

| Pin | Signal | Type | Drive | Description |
|---|---|---|---|---|
| **1** | ADDR4 | O | 4mA U | |
| **2** | ADDR5/TCK | O/I | 4mA U | **ADDR[5..9] are multiplexed** |
| **3** | ADDR6/TMS | O/I | 4mA U | **With JTAG functionality** |
| **4** | ADDR7/TDI | O/I | 4mA U | **Controlled by** |
| **5** | ADDR8/TDO | O/O | 4mA U | **LEDLNK/SEL signal** |
| **6** | ADDR9/TRST# | O/I | 4mA U | |
| **7** | PORTA0 | I/O | 2mA U | GPIO |
| **8** | PORTA1 | I/O | 2mA U | GPIO |
| **9** | PORTA2 | I/O | 2mA U | GPIO |
| **10** | PORTA3 | I/O | 2mA U | GPIO |
| **11** | PORTA4 | I/O | 2mA U | GPIO |
| **12** | PORTA5 | I/O | 2mA U | GPIO |
| **13** | PORTA6 | I/O | 2mA U | GPIO |
| **14** | PORTA7 | I/O | 2mA U | GPIO |
| **15** | PORTC0 | I/O | 2mA U | GPIO |
| **16** | PORTC1 | I/O | 2mA U | GPIO |
| **17** | SDA | O | 2mA U | Hardwired - I2C data signal |
| **18** | PORTC3 | I/O | 2mA U | GPIO |
| **19** | PORTC4 | I/O | 2mA U | GPIO |
| **20** | PORTC5 | I/O | 2mA U | GPIO |
| **21** | SCL | I/O | 2mA U | Hardwired - I2C clock signal |
| **22** | PORTC7 | I/O | 2mA U | GPIO |
| **23** | 3.3V | P | | 3.3V Power Connection |
| **24** | GND | P | | Ground Connection |

| | | | | |
|---|---|---|---|---|
| **25** | RESET# | I/O | 5mA U | Reset (bidirectional) |
| **26** | TPIP | I | | Ethernet Input+ |
| **27** | TPIN | I | | Ethernet Input- |
| **28** | TPOP | O | | Ethernet Output+ |
| **29** | TPON | O | | Ethernet Output- |
| **30** | LEDLNK/SEL# | O | | Ethernet Activity LED;<br>ADDR/JTAG Selection: |
| **31** | USB- | I/O | | Reserved |
| **32** | USB+ | I/O | | Reserved |
| **33** | DATA31 | I/O | 4mA | External data line D7 |
| **34** | DATA30 | I/O | 4mA | D6 |
| **35** | DATA29 | I/O | 4mA | D5 |
| **36** | DATA28 | I/O | 4mA | D4 |
| **37** | DATA27 | I/O | 4mA | D3 |
| **38** | DATA26 | I/O | 4mA | D2 |
| **39** | DATA25 | I/O | 4mA | D1 |
| **40** | DATA24 | I/O | 4mA | D0 |
| **41** | ADDR0 | O | 4mA U | Address Line |
| **42** | ADDR1 | O | 4mA U | Address Line |
| **43** | ADDR2 | O | 4mA U | Address Line |
| **44** | ADDR3 | O | 4mA U | Address Line |
| **45** | WE# | O | 4mA | Write Enable |
| **46** | OE# | O | 4mA | Output Enable |
| **47** | CS3# | O | 4mA | Chip Select 3 |
| **48** | CS4# | O | 4mA | Chip Select 4 |

The “U” in the Drive column denotes a pull-up resistor is present on this signal.

## 5. GPIO Configuration of UNC20

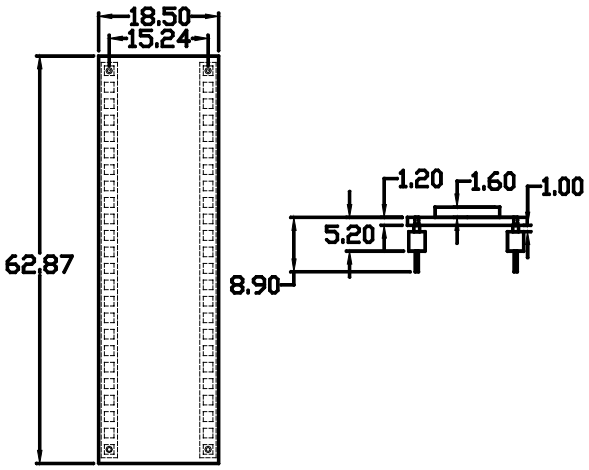
| GPIO | Serial | OTHER | PIN | | Serial | OTHER |
|---|---|---|---|---|---|---|
| A7 | TxDA | | 14 | I/O | Port A TxD | |
| A6 | DTRA_ | DREQ1_ | 13 | I/O | Port A DTR_ | DMA Chnl 3/5 Req |
| A5 | RTSA_ | | 12 | I/O | Port A RTS_ | |
| A4 | RxCA / RIA_ / OUT1A_ | | 11 | I/O | Pgmbl Out / Port A RxCLK / Port A Ring Signal / Port A SPI Clock (CLK) | |
| A3 | RxDA | DACK1_ | 10 | I/O | Port A RxD | DMA Chnl 3/5 Ack |
| A2 | DSRA_ | AMUX | 9 | I/O | Port A DSR_ | DRAM Addr Mux / USB Pwr Relay Ctrl |
| A1 | CTSA_ | DONE1_ (O) | 8 | I/O | Port A CTS_ | DMA Chnl 3/5 Done_Out |
| A0 | TxCA / OUT2A_ / DCDA_ | DONE1_ (I) | 7 | I/O | Pgmbl Out / Port A DCD / Port A SPI Enable (SEL_) / Port A TxCLK | DMA Chnl 3/5 DONE_ In |

| | | | | | | |
|---|---|---|---|---|---|---|
| C7 | TxDB | | 22 | I/O | Port B TXD | GEN Intrpt Out |
| C6 | DTRB_ | DREQ2_ | 21 | I/O | Port B DTR_ | DMA Chnl 4/6 Req<br><br>**I2C clock signal (SCL**) |
| C5 | RTSB_ | REJECT_ | 20 | I/O | Port B RTS_ | CAM Reject |
| C4 | RxCB / RIB_ / OUT1B_ | RESET_ / | 19 | I/O | Pgmbl Out / Port B RxCLK / Port B Ring Signal / Port B SPI Clock (CLK) | RESET Output |
| C3* | RxDB | LIRQ3 / DACK2_ | 18 | I/O | Port B RxD | Level Sensitive IRQ / DMA Chnl 4/6 Ack |
| C2* | DSRB_ | LIRQ2 / RPSF_ | 17 | O | Port B DSR_ | Level Sensitive IRQ / CAM Request<br><br>**I2C data signal (SDA**) |
| C1* | CTSB_ | LIRQ1 / DONE2_ (O) | 16 | I/O | Port B CTS_ | Level Sensitive IRQ / DMA Chnl 4/6 Done_Out |
| C0* | TxCB / OUT2B_ / DCDB_ | LIRQ0 / DONE2_ (I) | 15 | I/O | Pgmbl Out / Port B DCD / Port B SPI Enable (SEL_) / Port B TxCLK | Level Sensitive IRQ / DMA Chnl 4/6 DONE_ In |

## 6. Temperature and Power Specifications

| Characteristic | Min | Max | Unit |
|---|---|---|---|
| Operating Temperature (Ambient) | 0 | 70 | Degrees C |
| Storage Temperature | -50 | 125 | Degrees C |
| Power Consumption (at 3.3V) | 90 | 280 | mA |

## 7. Mechanical Information




All dimensions in mm.