ConnectCore 9c Hardware Reference

Making DEVICE NETWORKING easy™

ConnectCore™ 9C Hardware Reference

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Contents

Changes

This section lists the significant changes that have been made in the *ConnectCore 9C Hardware Reference* since the release of Rev. A of the manual (90000722_A). The current release is Rev. B.

The page numbers listed are the pages in the actual document, not the PDF page numbers.

General:
Changed RS232 to EIA-232 and changed RS485 to EIA-485 throughout the document, to match other, simialr Digi product documentation.

Chapter 1, About the Module

- Page 27: Pin 106 changed from No connect to Ethernet ACT_LED~.
- Page 27: Pin 108 changed from No connect to Ethernet LINK_LED5.

Chapter 2, About the Development Board

- Page 30: Replaced development board figure with updated drawing. A new switch was added above circle17 — circle 20, power toggle switch (SW23).
- Page 30: Switch 18 is annotated as circle 21 in the development board figure.
- Page 31: Added #20, SW23, and #21, SW18 to the development board description (What's on the development board).
- Page 31: Added new color identifiers for pins P8 (blue), P7 (black), and P16 (white).
- Pages 33, 34, and 35: Changed Pin 11 signal name *UBUFFENR~* to *B_UBUFFENR~ (optional)*.

- Page 36: Changed Pin 5 signal name *UBUFFENR~* to *B_UBUFFENR~ (optional)*.
- Page 39: Corrected incorrect pin descriptions for LCD backlight header connector, P9:
  - LCD_BLK_PWR → GND
  - LCD_BLK_PWR → GND
  - GND → LCD_BLK_PWR
  - GND → LCD_BLK_PWR
  - Not used → BRTL (luminance control)
  - Not used → BRTH (luminance control)
- Page 41: Corrected incorrect pin descriptions for touch interface screen connector, P13:
  - Pin 2 — Y+ → X-
  - Pin 3 — X- → Y+
- Page 43: Replaced the Serial Port A, P22 pin assignment table with a new table that describes EIA-422/485 signals.
- Page 44: Added SW 18 switch diagram and switch assignment table to the Serial Port A, P22 section.
- Page 45: Combined the information for serial ports B, C, and D as pin assignment and orientation are the same for all three.
- Page 49, Sockets:
  - Corrected AMP part number for SO-DIMM socket and added color identifier.
  - Added AMP part number for logic analyzer module/application kit module and added color identifier.
  - Updated the exception pins in the first paragraph of the section, adding 106 and 108 to the list.
- Pages 67–76, GPIO channel descriptions:
  - Deleted *N/R Not recommended* from the Legend at the beginning of the section.
  - In tables, in Signal path column, changed all instances of *terminate to ground* to *N/C*.

- In tables, where changed *terminate to ground*, changed the NS9360 function to *Localized*.
- Deleted notes 1, 2, 3, 6, 7, 9, 11, and 12 from the Table notes after GPIO channel 49. Renumbered the notes accordingly within the channel description tables as well as in the Table notes section.

- Page 79, Jumper 17 drawing: Changed SW18 to an 8-position dip switch rather than a 4-position dip switch. Decreased the size of the switch to reflect the size on the development board.
- Pages 81: Replaced the *Serial Ports* LED locations drawing with an updated drawing.
- Pages 81: Replaced the *Serial Ports* LED tables with explanatory text.
- Page 82: Replaced the *Power and I^2C* LED locations drawing with an updated drawing.
- Page 83: Replaced the *GPIO terminal strip P1* LED locations drawing with an updated drawing.
- Page 85: Replaced *GPIO terminal strip P2* LED locations drawing with an updated drawing.
- Page 86: Replaced the *GPIO terminal strips P3 and P5* LED locations drawing with an updated drawing.
- Page 87: Added a new section for the main power switch, SW23.
- Page 88: Corrected incorrect test point descriptions:
  - TP34 — GPIO-38 → GPIO-46
  - TP35 — GPIO-45 → GPIO-49
  - TP36 — GPIO-46 → GND

Chapter 3, LCD and USB Considerations

- Page 91: Added reference to the "LCD Displays Supported by the NetSilicon NS9750/NS9360 Processors" Application Note available on the Web. This Application Note provides additional information about the ConnectCore 9C LCD controller.
- Page 94: Changed SGA 800 x 800 to SVGA 800 x 600.
- Page 94: Removed XGA from list of supported resolutions.
- Page 97: Updated USB configuration drawing.

Appendix A, ConnectCore 9C Module Specifications
Page 110: Updated the PCB layout pin location drawing, to include additional dimension data.

Index
Updated index for SW18 and SW23.

Using This Guide

Review this section for basic information about the guide you are using, as well as general support and contact information.

About this guide

This guide provides information about the Digi ConnectCore 9C, an embedded core module for main processor applications.

The module design is based on the advanced and powerful 32-bit processor NS9360 with ARM926EJ-S core that is part of the award-winning family of NetSilicon NET+ARM System-on-Chip (SoC) solutions.

What's in this guide

This table shows where you can find specific information in this guide.

To read about	See
ConnectCore 9C module	Chapter 1, "About the ConnectCore 9C Module"
ConnectCore 9C development board	Chapter 2, "About the ConnectCore 9C Development Board"

To read about	See
ConnectCore 9C-specifics for the LCD and USB interfaces	Chapter 3, “LCD and USB Considerations”
Module specifications	Appendix A, “ConnectCore 9C Module Specifications

Conventions used in this guide

This table describes the typographic conventions used in this guide:

This convention	Is used for
italic type	Emphasis, new terms, variables, and document titles.
`monospaced type`	Filenames, pathnames, and code examples.

Related documentation

- *NS9360 Hardware Reference* provides detailed information about the NS9360 chip and interface modules. The *NS9360 Hardware Reference* is available in two versions: as one document online (or from your CD) — *90000675_A* — or as two printed volumes — *90000710_A* (Vol 1) and *900000711_A* (Vol 2).

Review the CD-ROM that came with your development kit for ConnectCore 9C development board schematics.

Documentation updates

Digi occasionally provides documentation updates on the Web site (www.digi.com/support).

Be aware that if you see differences between the documentation you received in your package and the documentation on the Web site, the Web site content is the latest version.

Customer support

To get help with a question or technical problem with this product, or to make comments and recommendations about our products or documentation, use the contact information listed in this table:

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About the Module

CHAPTER 1

This chapter provides an overview of the ConnectCore 9C, a highly-integrated, embedded core processor module in a compact and universal SO-DIMM (Small Outline Dual Inline Memory Module) form factor. The ConnectCore 9C provides core processing functionality with integrated network connectivity and a complete set of peripheral options.

What is the ConnectCore 9C module?

The ConnectCore 9C module is built on NetSilicon 32-bit NET+ARM technology, and provides these capabilities:

- Allows original equipment manufacturers to design in main processor functionality and networking capabilities with a single, high-performance solution.
- Delivers embedded networking connectivity while providing additional main processor performance and bandwidth to handle sophisticated embedded applications in applications such as building automation systems, POS systems, RFID readers, medical devices, instrumentation, networked displays, transportation systems, and industrial automation systems.
- Provides a seamless migration path to a fully integrated system-on-chip solution. Based on the NetSilicon NET+Works® development platform, the ConnectCore 9C core module delivers a complete out-of-the-box solution for embedded software development. By providing all the integrated building blocks needed to quickly and cost-effectively create secure and fully network-enabled product solutions, the ConnectCore 9C minimizes design risk and significantly accelerates the overall embedded software process.

Module features: General

- 32-bit NS9360 processor
- ARM926EJ-S RISC core with DSP/Jazelle enhancements
- Compact SO-DIMM (Small Outline-Dual Inline Memory Module) design
- Low power consumption
- Sleep mode power management
- Industrial operating temperature
- 4 MB flash, 16 MB RAM integrated
- 10/100 Mbit Ethernet interface with on-board RJ-45 connector
- 802.3af compliant power pass-through (mid-span and end-span)
- Up to four high-speed serial ports
  - UART and SPI mode configurable
- I^2C bus interface
- USB 1.1/2.0 compliant host/device interface
- On-board USB host connector option
- Integrated LCD controller
- Up to eight independent 16-/32-bit programmable timers, counters, or four PWM functions
- Four programmable external interrupts
- Up to 55 shared General Purpose Input/Output (GPIO) ports
  - Up to seven high-current (8mA) pins
- Real Time Clock
  - Processor powered, no battery backup
- Population options available (processor speed, memory, connectors)

Module features: Specific

Processor

The base module uses the industrial grade NS9360 processor running at 155 MHz.

Memory

4 MB Flash and 16 MB SDRAM are the module's standard configurations.

Interface features

Ethernet

The ConnectCore 9C module provides a 10/100 Mbps Ethernet interface with on-board RJ-45 connector and integrated LEDs.

- Full-duplex or half-duplex
- Station, broadcast, or multicast address filtering
- 2 kB RX FIFO
- 256-byte TX FIFO with on-chip buffer descriptor ring
- Separate TX and RX DMA channels
- Intelligent receive-side buffer size selection
- Full statistics gathering support
- External CAM filtering support

USB 2.0 Host/Device

- USB v2.0 full speed (12 Mbps) and low speed (1.5 Mbps)
- Independent OHCI Host and Device ports
- Internal USB PHY
- External USB PHY interface

- USB device supports one bidirectional endpoint and ten unidirectional endpoints
- All endpoints supported by a dedicated DMA channel
- 32 byte FIFO per endpoint

The ConnectCore 9C provides a population option for a one-to-four hub with onboard double-connector (500mA, 5V only) and full speed/low speed support.

Serial ports

- Four serial modules, each independently configurable to UART mode, SPI master mode, or SPI slave mode
- Bit rates from 75 bps to 921.6 kbps: asynchronous x16 mode
- Bit rates from 1.2 kbps to 11.25 Mbps: synchronous mode
- UART provides:
  - High performance hardware and software flow control
  - Odd, even, or no parity
  - 5, 6, 7, or 8 bits
  - 1 or 2 stop bits
  - Receive-side character and buffer gap timers
- Four receive-side data match detectors
- Two dedicated DMA channels per module, 8 channels total
- 32 byte TX FIFO and 32 byte RX FIFO per module

I^2C port

- I^2C v.1.0 configurable to master or slave
- Bit rates: fast (400 kHz) or normal (100 kHz) with clock stretching
- 7-bit and 10-bit address modes
- Supports I^2C bus arbitration

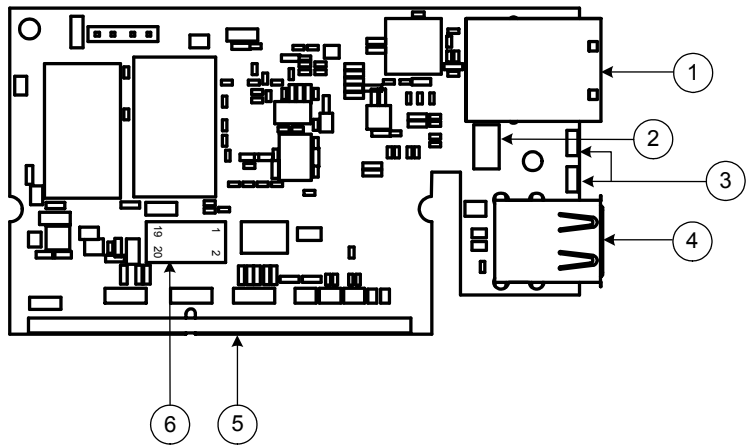
LCD controller

- Dual 64-deep, 32-bit wide FIFOs, for buffering incoming display data
- Support for color and monochrome single- and dual-panel for Super Twisted Nematic (STN) displays with 4- or 8-bit interfaces
- Support for Thin Film Transistor (TFT) color displays
- Resolution programmable up to 1024 x 768
- 15 gray-level mono, 3375 color STN, and 64K color TFT support
  - Patented gray-scale algorithm
- 1, 2, or 4 bits-per-pixel (bpp) palettized displays for mono STN
- 1, 2, 4, or 8 bpp palettized color displays for STN and TFT
- 16 bpp true-color non-palettized, for color STN and TFT
- Programmable timing for different display panels
- 256 entry, 16-bit palette RAM, arranged as a 128 x 32-bit RAM
- Frame, line, and pixel clock signals
- AC bias signal for STN, data enable signal for TFT panels
- Support for multiple data formats

Basic description

The module contains a fully 802.3af compliant Power-over-Ethernet (PoE) pass-through socket, connectors, Ethernet and USB ports, and LEDs that you use when integrating the ConnectCore 9C module into your design.

This figure shows the layout of the module.



What's on the module?

#	Description
1	Ethernet port
2	802.3af PoE pass-through header, P5
3	LEDs, CR1 and CR2. **CR1** = General purpose LED connected to GPIO66. Default is Off. Setting to output a logic "0" turns on the LED. When associated with the development board, see "Pin assignment by GPIO" on page 50. **CR2** = General purpose LED connected to GPIO67. Default is off. Setting to output logic "0" turns on LED. When associated with the development board, see "Pin assignment by GPIO" on page 50.
4	USB Host port. Optional. (See "USB interface signals" on page 102.)
5	SO-DIMM edge connector, P3. This is the side of the module that plugs into the development board at P16.
6	JTAG connector, P2

Configuration diagrams

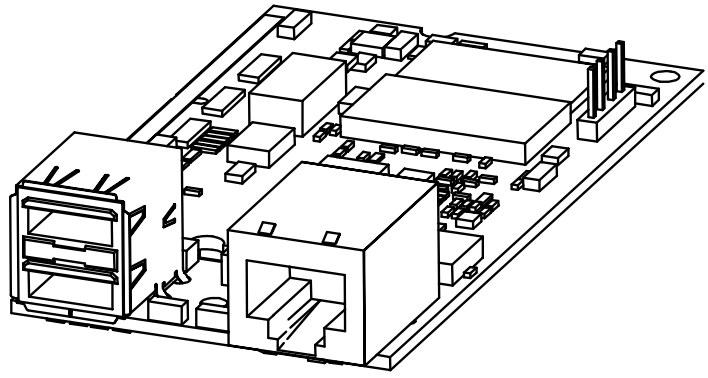
The ConnectCore 9C module is available in these two base configurations:

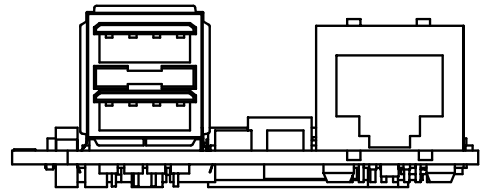
- With both USB and Ethernet interfaces
- With Ethernet interface only

Note: The development kit provides a module with the Ethernet interface only.

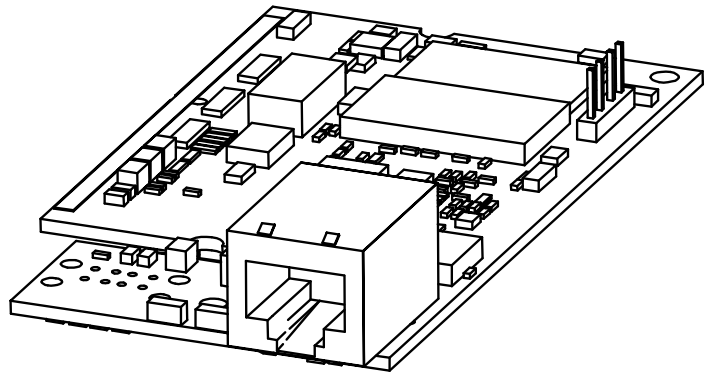
Each configuration is illustrated, top and edge views, in this section.

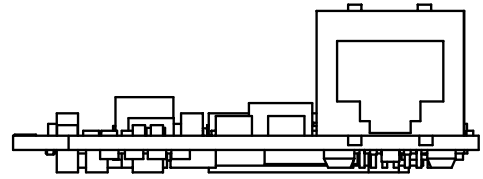
ConnectCore 9C module with Ethernet and USB





ConnectCore 9C module with Ethernet only





Additional population options are available. Please contact your local Digi sales office or distributor for information.

Connectors: Ethernet with LEDs

The Ethernet connector is an 8-wire RJ-45 jack with integrated magnetics that meets the ISO 8877 requirements for 10/100BASE-T. There are eight pins in the upper portion of the connector; these pertain to the Ethernet interface and are described in "Ethernet pin assignments" on page 10. There are two integrated LEDs in the lower portion of the connector; these are described in "LEDs" on page 12.

Pin orientation

Ethernet pin assignments

Pin	Signal	Description
1	TXD +	Transmit data +
2	TXD-	Transmit data-
3	RXD +	Receive data +
6	RXD-	Receive data -

802.3af pin assignments

Pin	End-Span (Mode A)	Mid-Span (Mode B)
1	Positive V_{Port}, Negative V_{Port}	
2	Positive V_{Port}, Negative V_{Port}	
3	Negative V_{Port}, Positive V_{Port}	
4		Positive V_{Port}, Negative V_{Port}
5		Positive V_{Port}, Negative V_{Port}
6	Negative V_{Port}, Positive V_{Port}	
7		Negative V_{Port}, Positive V_{Port}
8		Negative V_{Port}, Positive V_{Port}

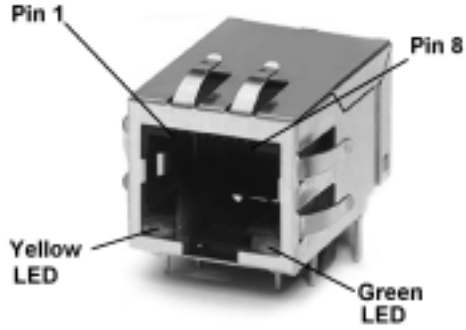
PoE support

If you are planning to add PoE support to your product, see the most recent revision of the IEEE 802.3af specification available at http://standards.ieee.org/getieee802/802.3.html. The document provides detailed information about the standard and its proper implementation.

The schematics included with the ConnectCore 9C development board provide a reference design for a 802.3af compliant power supply.

LEDs

The module has two LEDs that are located near the lower corners of the Ethernet port.



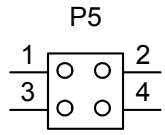
LED	Description
Yellow	Network activity: On when network traffic detected; Off when no network traffic detected.
	Diagnostic: flashes three times in even duration during powerup or reset, indicating successful startup.
Green	Network link: Optional. On indicates an active network link; Off indicates that no network link is present.

Connectors: PoE 4-pin header, P5

802.3af PoE (Power over Ethernet) pass-through socket: AMP, HDR, STR Dual Row p/n: 103186-2 and 103240-2

P5 mates with P18 header on the development board, which has a 48V to 5VDC, 2.5A isolated power supply. When power is supplied by an external 5DC power supply connected to P6, the PoE supply on the development board is automatically disabled.

Socket orientation and description



HDR2X2
00480004

Pin	Signal
1	POERCT
2	POETCT
3	POEA
4	POEB

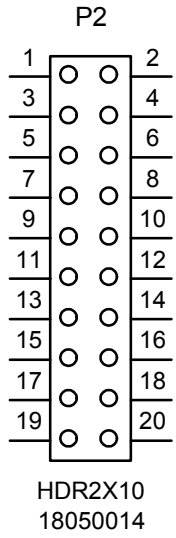
POERCT and POETCT connect to the P4 transformer CT (center tap) pair.

POEA and POEB connect to the Ethernet connector pin pairs 4/5 and 7/8 pair.

Connectors: JTAG 20-pin header connector, P2

The JTAG connector is a miniature connector, with a 50-mil pitch. A JTAG adapter, which ships with each development kit, expands the JTAG connector to a 100 mil pitch. If you want to interface the module with the debugger (for example, Raven), you need to use the adapter.

Pin orientation and description



Pin	Signal	Pin	Signal
1	VCC + (3.3V)	2	VCC + (3.3V)
3	TRST ~	4	GND
5	TDI	6	GND
7	TMS	8	GND
9	TCK	10	GND
11	RTCK	12	GND
13	TDO	14	GND
15	DBSRST ~	16	GND
17	n/a	18	GND
19	n/a	20	GND

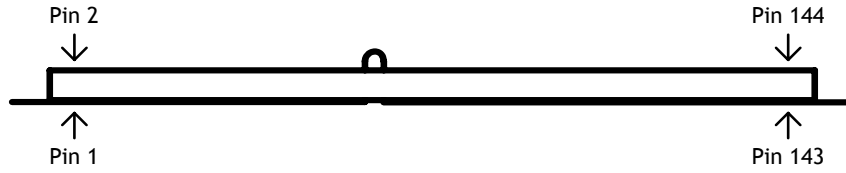
Connectors: Edge connector, P3

P3 mates with P16 (144-position SO-DIMM socket) on the development board. The pin orientation and description are on the next page. The first table shows information for all pins on the edge connector, in Dimm pin order. The remaining tables in the section are smaller for easier access to the information in the larger table, grouped by GPIO, other (power, USB, boot, reset), and reserved.

Some values are muxed to two different GPIO pins, to maximize the number of possible applications. The primary/duplicate signals are marked as such in the table. Selecting the primary GPIO pin and the duplicate pin for the same function is not recommended. See the NS9360 Hardware Reference for more information about pinouts and GPIO mux related options.

Note: The clearance underneath the module and development board should be 2.54mm (0.10”).

Pin orientation



Pin assignment by SO-DIMM pin number

Note: Functions with a superscripted 1 (for example, CLD10[1]) are duplicates. See the entries in the Notes column of the "Pin assignment by GPIO" table (on page 20) for details.

Dimm Pin	Signal	UART	SPI	I2C	USB	LCD	IEEE 1284	PWM	Timer	IRQ	BootStrap
1	GND										
2	GND										
3	+ 3.3V										
4	+ 3.3V										
5	+ 3.3V										
6	+ 3.3V										
7	Reserved										
8	BUFFENR ~										
9	Reserved										
10	Reserved										
11	Reserved										

Dimm Pin	Signal	UART	SPI	I2C	USB	LCD	IEEE 1284	PWM	Timer	IRQ	BootStrap
12	Reserved										
13	Reserved										
14	Reserved										
15	Reserved										
16	Reserved										
17	Reserved										
18	Reserved										
19	GND										
20	GND										
21	Reserved										
22	Reserved										
23	Reserved										
24	GPIO[71]			SDA							
25	Reserved										
26	GPIO[70]			SCL							
27	Reserved										
28	GPIO[69]									IRQ1	
29	GND										
30	GND										
31	GPIO[27]	DCD D	ENBL D			CLD3			TIMER4		
32	GPIO[68]										
33	GPIO[26]	RI D	CLK D			CLD2			TIMER3		
34	GPIO[67]										
35	GPIO[25]	DSR D				CLD1					
36	GPIO[66]										
37	GPIO[24]	DTR D				CLD0					CS1_MSB
38	GPIO[23]	DCD C	ENBL C			CLLE					
39	GND										
40	GND										
41	GPIO[47]	CTS D			RXD-		PINIT				
42	GPIO[22]	RI C	CLK C			CLAC					

Dimm Pin	Signal	UART	SPI	I2C	USB	LCD	IEEE 1284	PWM	Timer	IRQ	BootStrap
43	GPIO[46]	RTS D			RXD +		PAFD				
44	GPIO[21]	DSR C				CLFP					
45	GPIO[45]	RXD D	DIN D		RCV		PSTB				
46	GPIO[20]	DTR C				CLCP					CS1_LSB
47	GPIO[44]	TXD D	DOUT D		OE		PSELO				Endian
48	GPIO[43]	CTS C			DATA-		PDIR				
49	GND										
50	GND										
51	GPIO[38]					CLD14	PD7	PWM2			
52	GPIO[42]	RTS C			DATA +						
53	GPIO[36]					CLD12	PD5	PWM0			
54	GPIO[41]	RXD C	DIN C			CLD17					
55	GPIO[34]			SCL		CLD10	PD3				
56	GPIO[40]	TXD C	DOUT C			CLD16				IRQ3	
57	GPIO[32]					CLD8	PD1			IRQ2	
58	GPIO[39]					CLD15	PD8	PWM3			
59	GND										
60	GND										
61	GND										
62	GND										
63	GPIO[30]					CLD6 (CLD10)[1]			TIMER6		
64	GPIO[37]					CLD13	PD6	PWM1			
65	GPIO[28]					CLD4 (CLD8)[1]				IRQ1	
66	GPIO[35]			SDA		CLD11	PD4				
67	GPIO[15]	DCD A	ENBL A			LCDCLKI			TIMER2		
68	GPIO[33]					CLD9	PD2				
69	GPIO[14]	RI A	CLK A					PWM3	TIMER1		
70	GPIO[31]					CLD7 (CLD11)[1]			TIMER7		
71	GND										
72	GND										

Dimm Pin	Signal	UART	SPI	I2C	USB	LCD	IEEE 1284	PWM	Timer	IRQ	BootStrap
73	GPIO[13]	DSR A						PWM2		IRQ0	
74	GPIO[29]					CLD5 (CLD9)[1]			TIMER5		
75	GPIO[12]	DTR A						PWM1			ND3
76	GPIO[07]	DCD B	ENBL B							IRQ1	
77	GPIO[11]	CTS A							TIMER0	IRQ2	
78	GPIO[06]	RI B	CLK B				PFAULT		TIMER7		
79	GPIO[10]	RTS A						PWM0			ND2
80	GPIO[05]	DSR B					PERR				
81	GND										
82	GND										
83	GPIO[09]	RXD A	DIN A								
84	GPIO[04]	DTR B					PBUSY				ND0
85	GPIO[08]	TXD A	DOUT A								ND1
86	GPIO[03]	CTS B					PACK				
87	GPIO[19]					HSYNC					PLL_BYP
88	GPIO[02]	RTS B							TIMER0		FS1
89	GPIO[18]					CLPOWER				IRQ3	
90	GPIO[01]	RXD B	DIN B							IRQ0	
91	Reserved										
92	GPIO[00]	TXD B	DOUT B						TIMER1		FS0
93	GND										
94	GND										
95	Reserved										
96	GPIO[49]				SPD		PLH				CS_POL
97	Reserved										
98	GPIO[48]				SUSP		PSELI				
99	Reserved										
100	Reserved										
101	GND										
102	GND										
103	Reserved										

Dimm Pin	Signal	UART	SPI	I2C	USB	LCD	IEEE 1284	PWM	Timer	IRQ	BootStrap
104	Reserved										
105	MODRST ~										
106	Reserved										
107	Reserved										
108	Reserved										
109	GPIO[16]				OVRH ~		PFAULT	PWM0			
110	Reserved										
111	GPIO[17]				PONH ~						
112	Reserved										
113	OVR3 ~										
114	OVR4 ~										
115	PON3 ~										
116	PON4 ~										
117	OVR1 ~										
118	OVR2 ~										
119	PON1 ~										
120	PON2 ~										
121	GND										
122	GND										
123	DM4										
124	DP4										
125	GND										
126	GND										
127	DM3										
128	DP3										
129	GND										
130	GND										
131	DM2										
132	DP2										
133	GND										
134	GND										

Dimm Pin	Signal	UART	SPI	I2C	USB	LCD	IEEE 1284	PWM	Timer	IRQ	BootStrap
135	DM1										
136	DP1										
137	GND										
138	GND										
139	+5V										
140	+5V										
141	+5V										
142	+5V										
143	GND										
144	GND										

Pin assignment by GPIO

Signal	Dimm Pin	UART	SPI	I2C	USB	LCD	IEEE 1284	PWM	Timer	IRQ	Notes
GPIO[00]	92	TXD B	DOUT B						TIMER1		TIMER1: Primary on GPIO[14]
GPIO[01]	90	RXD B	DIN B							IRQ0	IRQ0: Duplicate on GPIO[13]
GPIO[02]	88	RTS B							TIMER0		TIMER0: Duplicate on GPIO[11]
GPIO[03]	86	CTS B					PACK				
GPIO[04]	84	DTR B					PBUSY				
GPIO[05]	80	DSR B					PERR				
GPIO[06]	78	RI B	CLK B				PFAULT		TIMER7		PFAULT: Primary on GPIO[16] TIMER7: Primary on GPIO[31]
GPIO[07]	76	DCD B	ENBL B							IRQ1	IRQ1: Duplicate on GPIO[28]
GPIO[08]	85	TXD A	DOUT A								

Signal	Dimm Pin	UART	SPI	I2C	USB	LCD	IEEE 1284	PWM	Timer	IRQ	Notes
GPIO[09]	83	RXD A	DIN A								
GPIO[10]	79	RTS A						PWM0			PWM0: Primary on GPIO[36]
GPIO[11]	77	CTS A							TIMER0	IRQ2	TIMER): Primary on GPIO[2] IRQ2: Primary on GPIO[23]
GPIO[12]	75	DTR A						PWM1			PWM1: Primary on GPIO[37]
GPIO[13]	73	DSR A						PWM2		IRQ0	IRQ0: Primary on GPIO[01] PWM2: Primary on GPIO[38]
GPIO[14]	69	RI A	CLK A					PWM3	TIMER1		TIMER1: Duplicate on GPIO[00] PWM3: Primary on GPIO[39]
GPIO[15]	67	DCD A	ENBL A			LCDCLKI			TIMER2		
GPIO[16]	109				OVRH ~		PFAULT	PWM)			OVRH ~ : USB overcurrent[2] PFAULT: Primary on GPIO[06] PWM): Duplicate on GPIO[10]
GPIO[17]	111				PONH ~						PONH ~ : USB power-on[2]
GPIO[18]	89					CLPOWER				IRQ3	IRQ3: Primary on GPIO[40]
GPIO[19]	87					HSYNC					
GPIO[20]	46	DTR C				CLCP					Output drive: 8mA
GPIO[21]	44	DSR C				CLFP					
GPIO[22]	42	RI C	CLK C			CLAC					
GPIO[23]	38	DCD C	ENBL C			CLLE					

Signal	Dimm Pin	UART	SPI	I2C	USB	LCD	IEEE 1284	PWM	Timer	IRQ	Notes
GPIO[24]	37	DTR D				CLD0					
GPIO[25]	35	DSR D				CLD1					
GPIO[26]	33	RI D	CLK D			CLD2			TIMER3		
GPIO[27]	31	DCD D	ENBL D			CLD3			TIMER4		
GPIO[28]	65					CLD4 (CLD8)[1]				IRQ1	CLD8: Primary on GPIO[32] IRQ1: Primary on GPIO[07]
GPIO[29]	74					CLD5 (CLD9)[1]			TIMER5		CLD9: Primary on GPIO[33]
GPIO[30]	63					CLD6 (CLD10)[1]			TIMER6		CLD10: Primary on GPIO[34]
GPIO[31]	70					CLD7 (CLD11)[1]			TIMER7		CLD11: Primary on GPIO[35] TIMER7: Duplicate on GPIO[06]
GPIO[32]	57					CLD8	PD1			IRQ2	CLD8: Duplicate on GPIO[28] IRQ2: Duplicate on GPIO[11]
GPIO[33]	68					CLD9	PD2				CLD9: Duplicate on GPIO[29]
GPIO[34]	55			SCL		CLD10	PD3				SCL: Duplicate on GPIO[70] CLD10: Primary on GPIO[30]
GPIO[35]	66			SDA		CLD11	PD4				SDA: Duplicate on GPIO[71] CLD11: Primary on GPIO{31]
GPIO[36]	53					CLD12	PD5	PWM0			PWM0: Duplicate on GPIO[10]
GPIO[37]	64					CLD13	PD6	PWM1			PWM1: Duplicate on GPIO[12]

Signal	Dimm Pin	UART	SPI	I2C	USB	LCD	IEEE 1284	PWM	Timer	IRQ	Notes
GPIO[38]	51					CLD14	PD7	PWM2			PWM2: Duplicate on GPIO[13]
GPIO[39]	58					CLD15	PD8	PWM3			PWM3: Duplicate on GPIO[14]
GPIO[40]	56	TXD C	DOUT C			CLD16				IRQ3	IRQ3: Duplicate on GPIO{18]
GPIO[41]	54	RXD C	DIN C			CLD17					
GPIO[42]	52	RTS C			DATA +						
GPIO[43]	48	CTS C			DATA-		PDIR				
GPIO[44]	47	TXD D	DOUT D		OE		PSELO				Endian: Pull down for Big Endian
GPIO[45]	45	RXD D	DIN D		RCV		PSTB				
GPIO[46]	43	RTS D			RXD +		PAFD				USB: RXD + only used for unidirectional PHY
GPIO[47]	41	CTS D			RXD-		PINIT				USB: RXD- only used for unidirectional PHY
GPIO[48]	98				SUSP		PSELI				
GPIO[49]	96				SPD		PLH				
GPIO[66]	36										CR1 Output drive: 8mA
GPIO[67]	34										MFGOCR2 Output drive: 8mA
GPIO[68]	32									IRQ0	IRQ0: Primary on GPIO[01] Output drive: 8mA
GPIO[69]	28									IRQ1	Output drive: 8mA IRQ1: Primary on GPIO[07]
GPIO[70]	26			SCL							Output drive: 8mA SCL: Primary on GPIO[34]

Signal	Dimm Pin	UART	SPI	I2C	USB	LCD	IEEE 1284	PWM	Timer	IRQ	Notes
GPIO[71]	24			SDA							Output drive: 8mA SDA: Primary on GPIO[35]

1 Functions are duplicates.

2 Available as GPIO on module with on-board USB and module with Ethernet-only if USB is not used.

Pin assignment by SO-DIMM, Power, USB, Boot, and Reset

Dimm Pin	Signal	Notes
105	MODRST ~	Hardware reset (input; active LOW; minimum pulse width 10µs)
8	BUFFENR ~	Output (active LOW); Hold user buffers off during powerup/down until signal active
117	OVR1 ~	USB port 1 overcurrent[3]
118	OVR2 ~	USB port 2 overcurrent[3]
113	OVR3 ~	USB port 3 overcurrent[3]
114	OVR4 ~	USB port 4 overcurrent[3]
119	PON1 ~	USB port 1 power-on[3]
120	PON2 ~	USB port 2 power-on[3]
115	PON3 ~	USB port 3 power-on[3]
116	PON4 ~	USB port 4 power-on[3]
3	+ 3.3V	
4	+ 3.3V	
5	+ 3.3V	
6	+ 3.3V	
139	+ 5V	Power to USB, if used[4]
140	+ 5V	Power to USB, if used[4]
141	+ 5V	Power to USB, if used[4]
142	+ 5V	Power to USB, if used[4]
135	DM1	USB port 1 data (-)[3]
131	DM2	USB port 2 data (-)[3]
127	DM3	USB port 3 data (-)[3]

Dimm Pin	Signal	Notes
123	DM4	USB port 4 data (-)[3]
136	DP1	USB port data (+)[3]
132	DP2	USB port 2 data (+)[3]
128	DP3	USB port 3 data (+)[3]
124	DP4	USB port data (+)[3]
1	GND	
2	GND	
19	GND	
20	GND	
29	GND	
30	GND	
39	GND	
40	GND	
49	GND	
50	GND	
59	GND	
60	GND	
61	GND	
62	GND	
71	GND	
72	GND	
81	GND	
82	GND	
93	GND	
94	GND	
101	GND	
102	GND	
121	GND	
122	GND	
125	GND	
126	GND	
129	GND	

Dimm Pin	Signal	Notes
130	GND	
133	GND	
134	GND	
137	GND	
138	GND	
143	GND	
144	GND	

3 Reserved for future use; no connect

4 Module with on-board USB

Pin assignment by SO-DIMM, Reserved pins

Dimm Pin	Signal	Notes
7	Reserved	No connect
9	Reserved	No connect
10	Reserved	No connect
11	Reserved	No connect
12	Reserved	No connect
13	Reserved	No connect
14	Reserved	No connect
15	Reserved	No connect
16	Reserved	No connect
17	Reserved	No connect
18	Reserved	No connect
21	Reserved	No connect
22	Reserved	No connect
23	Reserved	No connect
25	Reserved	No connect
27	Reserved	No connect
91	Reserved	No connect
95	Reserved	No connect

Dimm Pin	Signal	Notes
97	Reserved	No connect
99	Reserved	Ethernet TXB + R[5]
100	Reserved	Ethernet TXA + R[5]
103	Reserved	Ethernet TXB-R[5]
104	Reserved	Ethernet TXA-R[5]
106	Reserved	Ethernet ACT_LED ~
107	Reserved	No connect
108	Reserved	Ethernet LINK_LED5
110	Reserved	No connect
112	Reserved	No connect

5 Reserved for future use; no connect

About the Development Board

CHAPTER 2

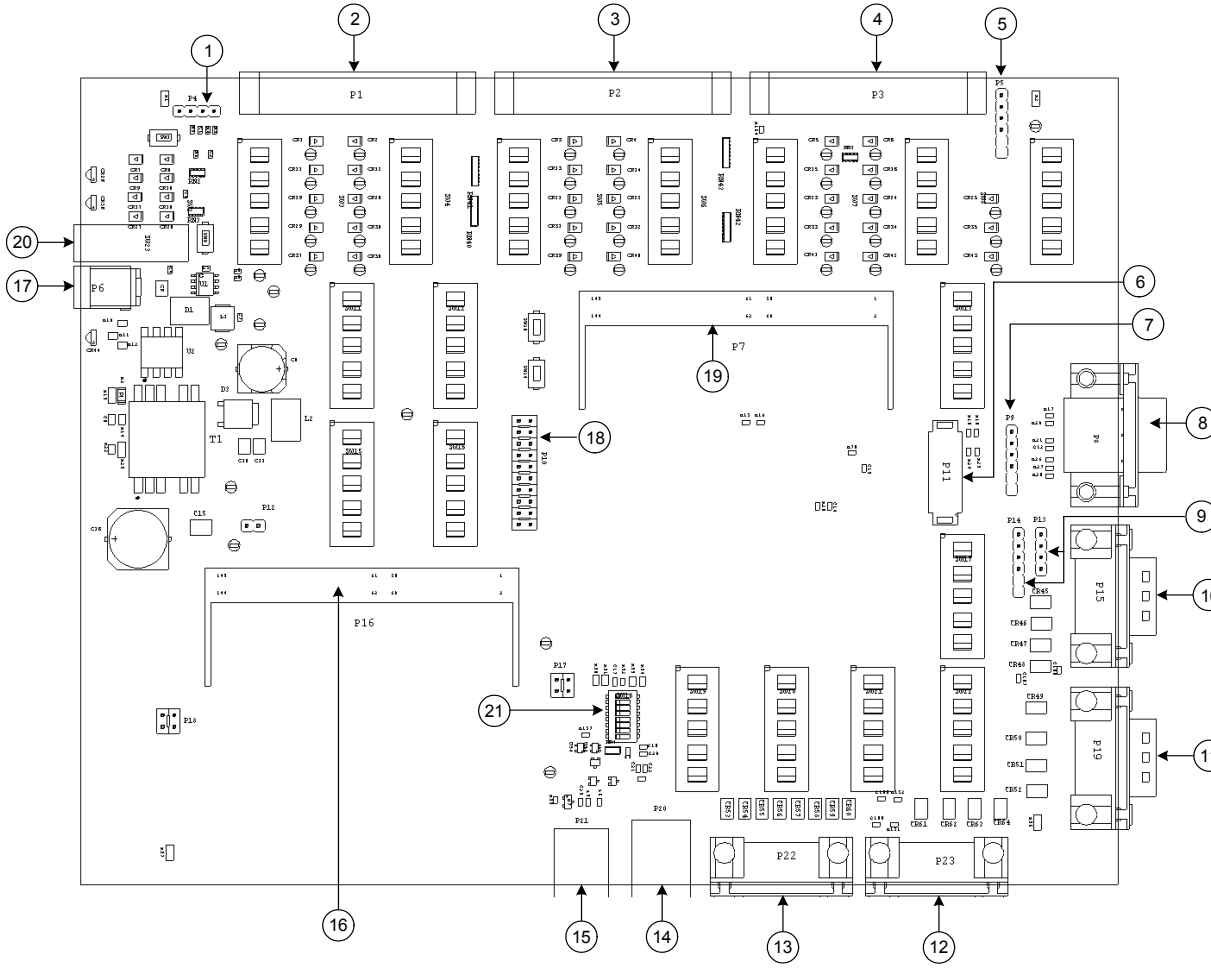
This chapter provides information for configuring the ConnectCore 9C development board, and details the development board's default and optional configuration states.

For more detailed information on the development board, see the schematics and mechanical drawings on the CD that comes with your development kit.

Basic description

The development board contains connectors, switches, and LEDs that you use when integrating the ConnectCore 9C module into your design. The board also provides test points; for more information about test points, see "Test points" on page 88.

This figure shows the location of the connectors and switches. The test points are not shown on the figure. LED conditions and sources are described in "Development board LEDs" on page 80.



What's on the development board?

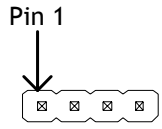
#	Description	#	Description
1	P4: I^2C connector	12	P23: Serial Port B
2	P1: GPIO connector bank 1	13	P22: Serial Port A
3	P2: GPIO connector bank 2	14	P20: USB Host
4	P3: GPIO connector bank 3	15	P21: USB Device
5	P5: Additional GPIO connector	16	P16: SO-DIMM socket for ConnectCore 9C module (white)
6	P11: LCD data connector	17	Barrel connector for external 5v power supply. See "Power jack" on page 87 for more information.
7	P9: LCD backlight	18	P10: I^2C GPIO expander
8	P8: VGA connector (blue)	19	P7:Socket for application kit/ Logic analyzer board (black)
9	P13: Touch Screen P14: SPI connector	20	SW23: Power toggle switch. Switch turns off power.
10	P15: Serial Port D	21	SW18: Serial Port A, EIA-232 or EIA-485/422 selection
11	P19: Serial Port C		

Warning: When handling the development board, wear a grounding wrist strap to avoid ESD damage to the board.

I²C header connector, P4

The development board has a 4-pin I²C header connector, labeled as P4.

Pin orientation



Pin assignment

Pin	Signal	Description
1	I2C_DAT	I²C data
2	+ 5V	+ 5V
3	I2C_CLK	I²C clock
4	GND	Ground

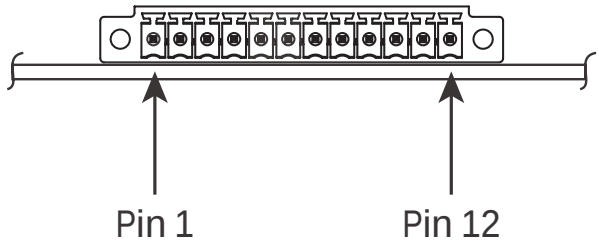
GPIO connector banks

The GPIO connector bank is a 12-pin male right-angle connector. The development board has three GPIO connector banks — labeled P1, P2, and P3— as well as an additional GPIO connector labeled P5.

Note: The development board is shipped with a 12-pin screw-flange plug attached to the GPIO port.

GPIO connector bank 1, P1

Pin orientation

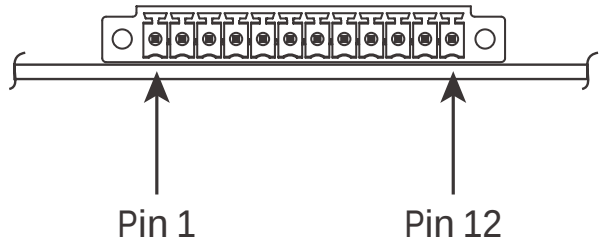


Pin assignment Bank 1

Pin	Signal name	Pin	Signal name
1	GPIO_0	7	GPIO_6
2	GPIO_1	8	GPIO_7
3	GPIO_2	9	GPIO_8
4	GPIO_3	10	GPIO_9
5	GPIO_4	11	B_UBUFFENR~ (optional)
6	GPIO_5	12	GND

GPIO connector bank 2, P2

Pin orientation

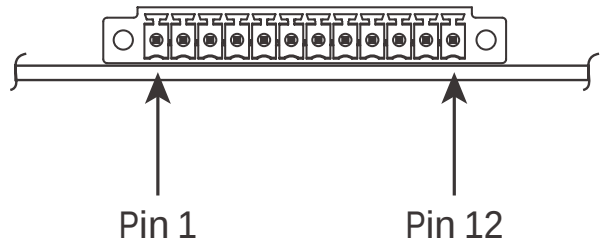


Pin assignment bank 2

Pin	Signal name	Pin	Signal name
1	GPIO_10	7	GPIO_23
2	GPIO_11	8	GPIO_32
3	GPIO_12	9	GPIO_33
4	GPIO_13	10	GPIO_34
5	GPIO_14	11	B_UBUFFENR ~ (optional)
6	GPIO_15	12	GND

GPIO connector bank 3, P3

Pin orientation

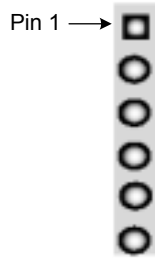


Pin assignment bank 3

Pin	Signal name	Pin	Signal name
1	GPIO_35	7	GPIO_43
2	GPIO_36	8	GPIO_44
3	GPIO_37	9	GPIO_45
4	GPIO_38	10	GPIO_46
5	GPIO_39	11	B_UBUFFENR~ (optional)
6	GPIO_42	12	GND

Additional GPIO connector, P5

Pin orientation



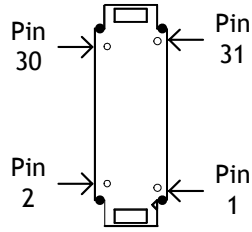
Pin assignment

Pin	Signal name
1	GPIO_47
2	GPIO_48
3	GPIO_49
4	Not connected
5	B_UBUFFENR~ (optional)
6	GND

LCD data connector, P11

The LCD data connector is a 31-pin, DF9-31 series connector. The development board has one LCD connector, labeled as P11.

Pin orientation



Pin assignment

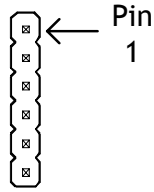
Pin	Signal	Description
1	GND1	Ground
2	CLK	B_LCD_CLOCK
3	HSYNC	B-LCD-HSYNC
4	VSYNC	B-LCD-VSYNC
5	GND2	Ground
6	R0	B_LCD_D[0]
7	R1	B_LCD_D[1]
8	R2	B_LCD_D[2]
9	R3	B_LCD_D[3]
10	R4	B_LCD_D[4]
11	R5	B_LCD_D[5]
12	GND3	Ground
13	G0	B_LCD_D[6]
14	G1	B_LCD_D[7]

Pin	Signal	Description
15	G2	B_LCD-D[8]
16	G3	B_LCD_D{9]
17	G4	B_LCD_D[10]
18	G5	B_LCD_D[11]
19	GND4	Ground
20	B0	B_LCD_D[12]
21	B1	B_LCD_D[13]
22	B2	B_LCD_D[14]
23	B3	B_LCD_D[15]
24	B4	B_LCD_D[16]
25	B5	B_LCD_D[17]
26	GND5	Ground
27	ENAB	B_LCD_BIAS_DATA_EN
28	LCD_VCC1	LCD_VCC
29	LCD_VCC2	LCD_VCC
30	R/L	Ground
31	U/D	Ground

LCD backlight header connector, P9

The development board has one 6-pin LCD backlight header connector, labeled as P9.

Pin orientation



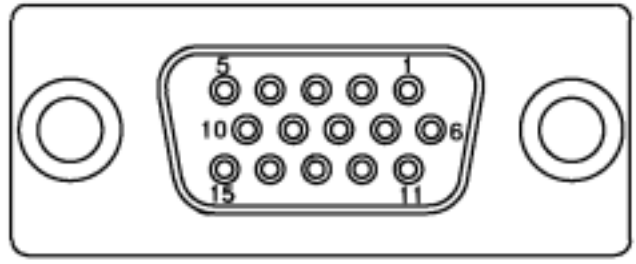
Pin assignment

Pin	Signal
1	GND
2	GND
3	LCD_BLK_PWR
4	LCD_BLK_PWR
5	BRTL (luminance control)
6	BRTH (luminance control)

VGA connector, P8

The VGA header is a 15-pin female connector. The development board has one VGA connector, labeled as P8.

Pin orientation



Pin assignment

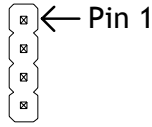
Signals marked with an asterisk (*) in this table are analog 0.7V p-p positive signals to 75 ohm load. All other signals are TTL level signals.

Pin	Description	Pin	Description
1	Red out *	2	Green out *
3	Blue out *	4	Monitor ID2 in
5	Ground	6	Red return
7	Blue return	8	Blue return
9	no pin	10	Sync return
11	Monitor ID0 in	12	Monitor ID1 in
13	Horizontal sync out	14	Vertical sync out
15	Reserved (monitor ID3)		

Touch interface screen connector, P13

The development board has one 4-pin touch screen interface connector, labeled as P13.

Pin orientation



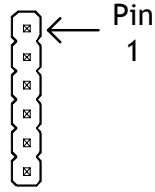
Pin assignment

Pin	Signal
1	X +
2	X-
3	Y +
4	Y-

SPI connector, P14

The development board has one 6-pin SPI header connector, labeled as P14.

Pin orientation



Pin assignment

Pin	Signal
1	+ 3.3V
2	SPI_DOUT [IO0]
3	SPI_DIN [IO1]
4	SPI_CLK [IO6]
5	SPI_CS0
6	GND

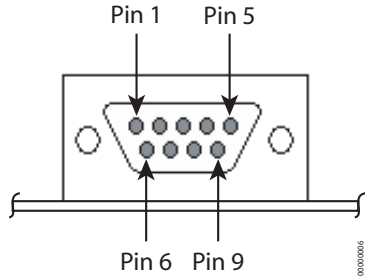
Serial port descriptions

The development board has four serial ports: A (P22), B (P23), C (P19), and D (P15). Each serial port is a DB-9 male connector.

Serial port A, P22

Switch 18 selects the signal modes (see page 44).

Pin orientation



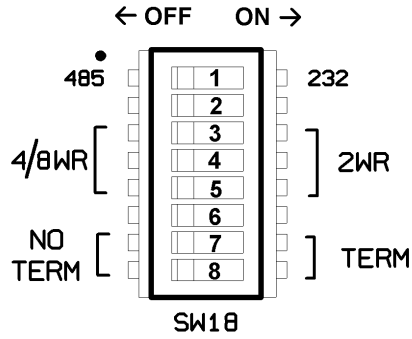
Pin assignment

Pin	EIA-232 signal	EIA-422/485 4/8-wire	EIA-485 2-wire	EIA-232 signal description
1	DCD	CTS- (B)		Data Carrier Detect
2	RXD	RXD + (A)	DATA + (A)	Receive Data
3	TXD	TXD + (A)		Transmit Data
4	DTR	RTS- (B)		Data Terminal Ready
5	GND	GND	GND	Ground
6	DSR	RXD- (B)	DATA- (B)	Data Set Ready
7	RTS	RTS + (A)		Request to Send
8	CTS	CTS + (A)		Clear to Send
9	RI	TXD- (B)		Ring Indicator
Shell is chassis GND.				

Switch 18

Switch 18 provides serial mode selection for serial port A (see page 43).

Switch orientation



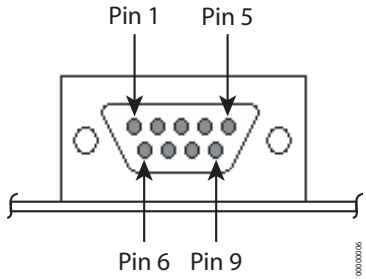
Switch assignment

	Switch settings							
EIA-mode	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**
232	ON	X	OFF	OFF	OFF	X	OFF	OFF
422/485, 4/8 Wire	OFF	X	OFF	OFF	OFF	X	T	T
485, 2 Wire	OFF	X	ON	ON	ON	X	T	T
X = Don't care; switches 2 and 6								
T = EIA-485 termination on if both switches 7 and 8 are ON								

Serial ports B (P23), C (P19), and D (P15)

The pin orientation and pin assignments for serial ports B, C, and D are the same.

Pin orientation



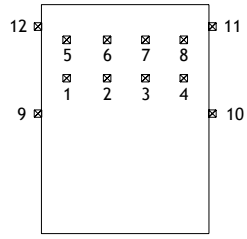
Pin assignment

Pin	Signal	Description
1	—	No connect
2	RXD	Receive Data
3	TXD	Transmit Data
4	—	No connect
5	GND	Ground
6	—	No connect
7	RTS	Request to Send
8	CTS	Clear to Send
9	—	No connect
Shell is chassis GND.		

USB Host connector, P20

The USB Host connector is a 12-pin USB type A dual connector. The development board has one USB Host connector, labeled as P20.

Pin orientation



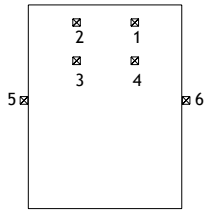
Pin assignment

Pin	Signal	Description
1	VCC_USB1	
2	D1M	
3	D1P	
4	GND	Ground
5	VCC_USB2	
6	D2M	
7	D2P	
8	GND	Ground
9	CGND	C Ground
10	CGND	C Ground
11	CGND	C Ground
12	CGND	C Ground

USB Device connector, P21

The USB Device connector is a 6-pin USB_B connector. The development board has one USB Device connector, labeled as P21.

Pin orientation



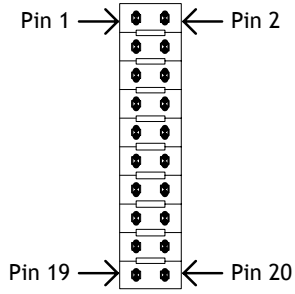
Pin assignment

Pin	Signal	Description
1	VCC	+ 5V
2	D-	
3	D +	
4	GND	Ground
5	SHIELD1	CGND
6	SHIELD2	CGND

I²C GPIO header connector, P10

The I²C GPIO header is a 20-pin connector. The development board has one I²C GPIO header connector, labeled as P10.

Pin Orientation



Pin assignment

Pin	Signal	Pin	Signal
1	P_I2C_GPIO_0	2	P_I2C_GPIO_1
3	P_I2C_GPIO_2	4	P_I2C_GPIO_3
5	P_I2C_GPIO_4	6	P_I2C_GPIO_5
7	P_I2C_GPIO_6	8	P_I2C_GPIO_7
9	P_I2C_GPIO_8	10	P_I2C_GPIO_9
11	P_I2C_GPIO_10	12	P_I2C_GPIO_11
13	P_I2C_GPIO_12	14	P_I2C_GPIO_13
15	P_I2C_GPIO_14	16	P_I2C_GPIO_15
17	No connect	18	No connect
19	GND	20	GND

Sockets

Development board SO-DIMM socket, P16
Logic analyzer module/Application kit module socket, P7

AMP part number: 390112-1 (SO-DIMM socket, white)

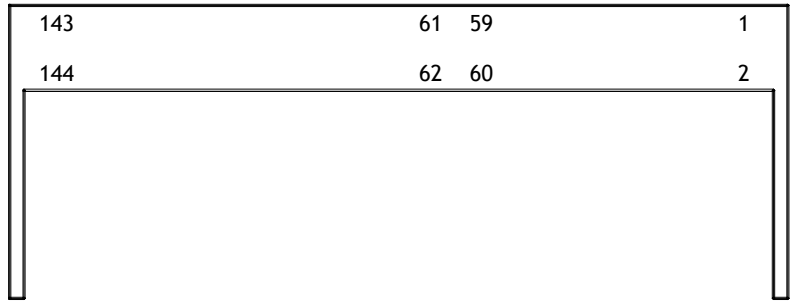
AMP part number: 7-390112-1 (logic analyzer module/application kit module, black)

The pinouts for the development board SO-DIMM socket (P16) and the logic analyzer module/application kit module socket (P7) are the same, with the exception of these pins: 99, 100, 101, 102, 103, 104, 106 and 108.

- You plug the ConnectCore 9C module into the P16 socket.
- You plug the optional logic analyzer board or available application kit modules into the P7 socket.

Note: The clearance underneath the module and development board should be 2.54mm (0.10”).

Pin orientation



Pin assignment by SO-DIMM pin number

See "Pin assignment by SO-DIMM pin number" on page 15.

Pin assignment by GPIO

See "Pin assignment by GPIO" on page 20.

Pin assignment by SO-DIMM, Power, USB, Boot, and Reset

See "Pin assignment by SO-DIMM, Power, USB, Boot, and Reset" on page 24.

Pin assignment by SO-DIMM, Reserved pins

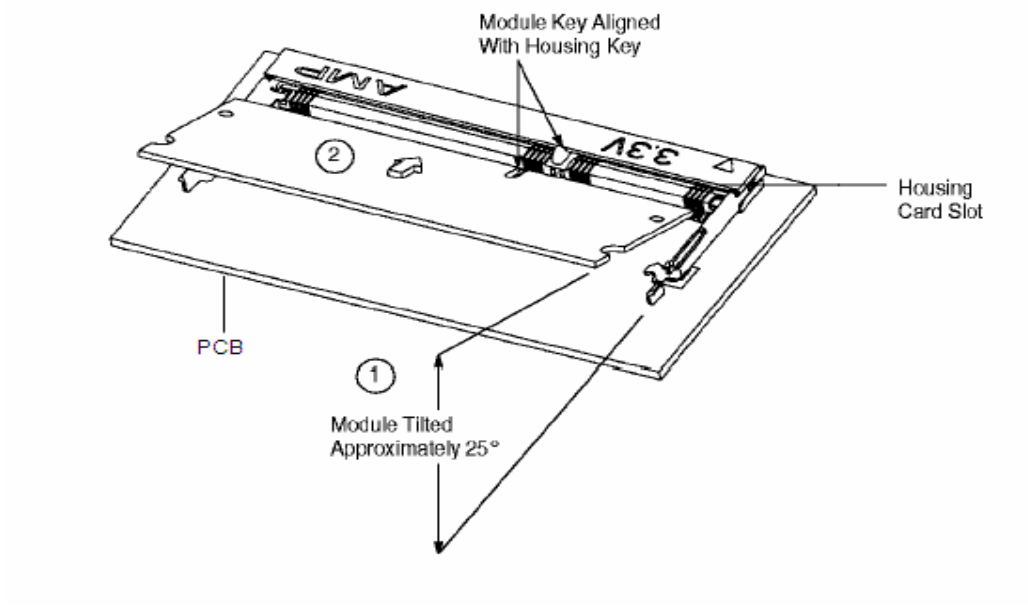
See "Pin assignment by SO-DIMM, Reserved pins" on page 26.

Inserting SO-DIMM modules

To ensure that you insert the SO-DIMM modules properly, review these steps and figures:

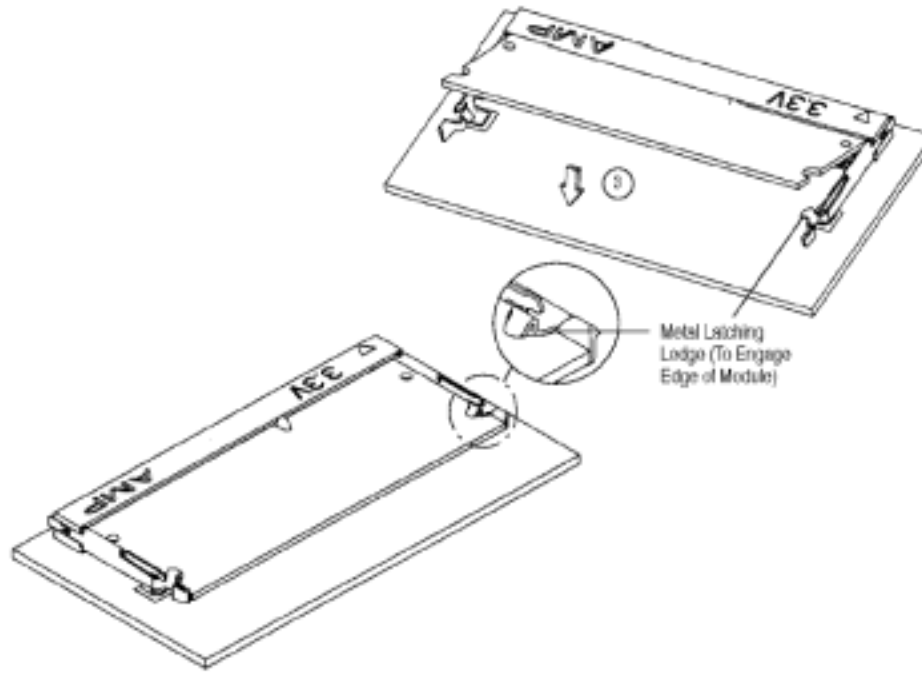
Step 1

Be sure the module key is aligned with the housing key.



Step 2

Be sure the metal latching edge engages the edge of the ConnectCore 9C module.

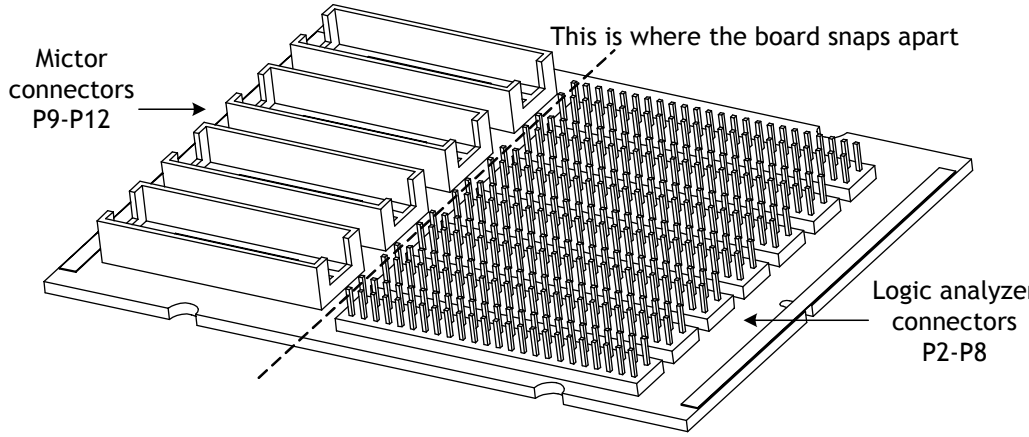


Logic analyzer adaptor

The logic analyzer adaptor board (DIGI part number: CC-9C-ACC-LAB) is an optional accessory item that brings out the signals that allow you to connect to a logic analyzer. The adaptor comes as one “board” that snaps into two pieces, each of which can be plugged into P7 (see "Basic description" on page 30). Each piece provides different functionality. Plug in the piece whose functionality you want to use.

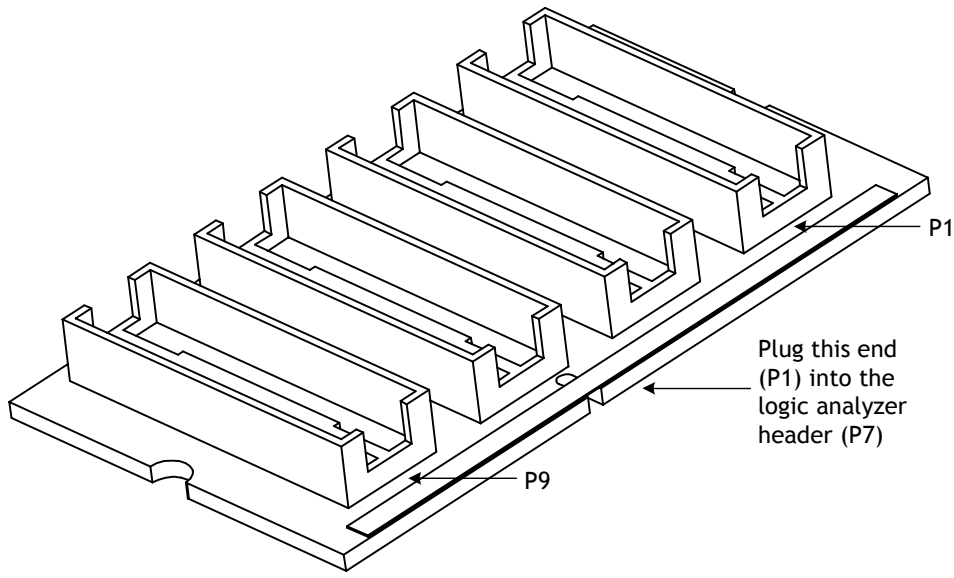
Logic analyzer single “board”

The two parts of the logic analyzer board are the Mictor connectors and the logic analyzer connectors. This figure shows the single board:



Mictor connectors

There are four 38-pin Mictor connectors as well as the connector that mates with P7 on the ConnectCore 9C development board. P1 is along the long edge and mates with P7. The other connectors — P9, P10, P11, and P12 — are shown in the next diagram and explained in the following table.



Signal name	Mictor connector pin number	ConnectCore 9C pin number
Mictor connector P9		
NC27	31	9
NC18	32	10
NC26	33	11
NC17	34	12
NC25	35	13
NC16	36	14
NC24	37	15

Signal name	Mictor connector pin number	ConnectCore 9C pin number
NC15	38	16
Mictor connector P10		
PWRDN ~	7	7
UBUFFEN ~	8	8
NC23	9	17
NC14	10	18
NC22	11	21
IO72	12	22
NC21	13	23
IO71	14	24
NC20	15	25
IO70	16	26
NC19	17	27
IO69	18	28
IO27	19	31
IO68	20	32
IO26	21	33
IO67	22	34
IO25	23	35
IO66	24	36
IO24	25	37
IO23	26	38
IO47	27	41
IO22	28	42
IO46	29	43
IO21	30	44
IO45	31	45

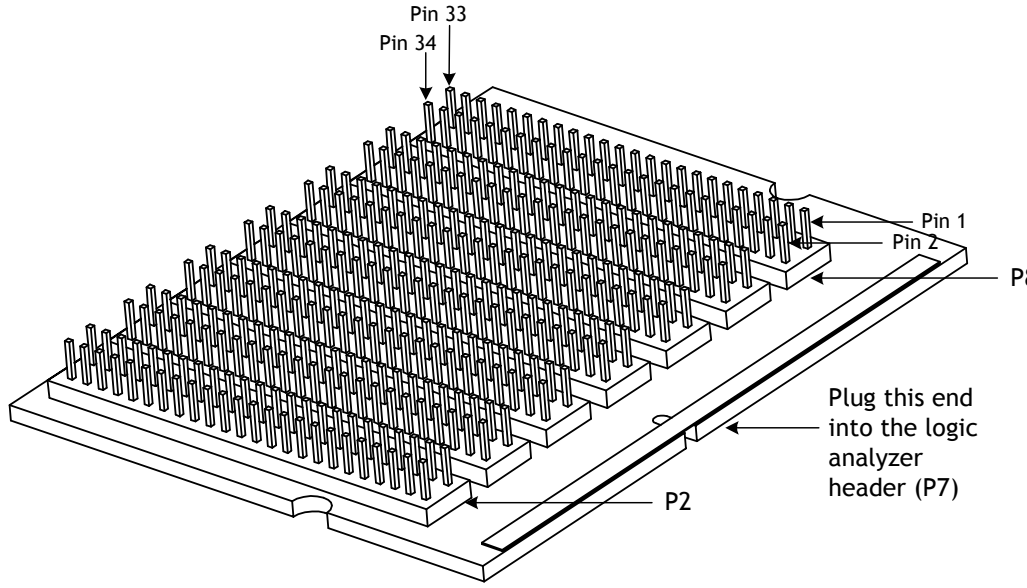
Signal name	Mictor connector pin number	ConnectCore 9C pin number
IO20	32	46
IO44	33	47
IO43	34	48
IO38	35	51
IO42	36	52
IO36	37	53
IO41	38	54
Mictor connector P11		
IO34	7	55
IO40	8	56
IO32	9	57
IO39	10	58
IO30	11	63
IO37	12	64
IO28	13	65
IO35	14	66
IO15	15	67
IO33	16	68
IO14	17	69
IO31	18	70
IO13	19	73
IO29	20	74
IO12	21	75
IO7	22	76
IO11	23	77
IO6	24	78
IO10	25	79

Signal name	Mictor connector pin number	ConnectCore 9C pin number
IO5	26	80
IO9	27	83
IO4	28	84
IO8	29	85
IO3	30	86
IO19	31	87
IO2	32	88
IO18	33	89
IO1	34	90
NC13	35	91
IO0	36	92
NC12	37	95
IO49	38	96
Mictor connector P12		
NC11	7	97
IO48	8	98
NC10	9	99
NC7	10	100
NC9	11	101
NC6	12	102
NC8	13	103
NC5	14	104
MODRST ~	15	105
NC4	16	106
BOOTMUX	17	107
NC3	18	108
IO16	19	109

Signal name	Mictor connector pin number	ConnectCore 9C pin number
NC2	20	110
IO17	21	111
NC1	22	112
OVR3 ~	23	113
OVR4 ~	24	114
PON3 ~	25	115
PON4 ~	26	116
OVR1 ~	27	117
OVR2 ~	28	118
PON1 ~	29	119
PON2 ~	30	120
DM4	31	123
DP4	32	124
DM3	33	127
DP3	34	128
DM2	35	131
DP2	36	132
DM1	37	135
DP1	38	136

Logic analyzer header connectors

There are six logic analyzer header connectors as well as the connector that mates with P7 on the ConnectCore 9C development board. P1 is along the long edge and mates with P7. The other connectors — P2, P3, P4, P45, P6, P7, and P8 — are shown in the next diagram and explained in the following table.



Note: Even connector pin numbers are GND.

Signal name	Logic analyzer header connector pin number	ConnectCore 9C pin number
Logic analyzer header connector P2		
NC27	17	9
NC18	19	10
NC26	21	11
NC17	23	12
NC25	25	13
NC16	27	14
NC24	29	15

Signal name	Logic analyzer header connector pin number	ConnectCore 9C pin number
NC15	31	16
Logic analyzer header connector P3		
NC23	1	17
NC14	3	18
PWRDN ~	5	7
UBUFFEN ~	7	8
NC22	9	21
IO72	11	22
NC21	13	23
IO71	15	24
NC20	17	25
IO70	19	26
NC19	21	27
IO69	23	28
IO27	25	31
IO68	27	32
IO26	29	33
IO67	31	34
Logic analyzer header connector P4		
IO25	1	35
IO66	3	36
IO24	5	37
IO23	7	38
IO47	9	41
IO22	11	42
IO46	13	43
IO21	15	44

Signal name	Logic analyzer header connector pin number	ConnectCore 9C pin number
IO45	17	45
IO20	19	46
IO44	21	47
IO43	23	48
IO38	25	51
IO42	27	52
IO36	29	53
IO41	31	54
Logic analyzer header connector P5		
IO34	1	55
IO40	3	56
IO32	5	57
IO39	7	58
IO30	9	63
IO37	11	64
IO28	13	65
IO35	15	66
IO15	17	67
IO33	19	68
IO14	21	69
IO31	23	70
IO13	25	73
IO29	27	74
IO12	29	75
IO7	31	76
Logic analyzer header connector P6		
IO11	1	77

Signal name	Logic analyzer header connector pin number	ConnectCore 9C pin number
IO6	3	78
IO10	5	79
IO5	7	80
IO9	9	83
IO4	11	84
IO8	13	85
IO3	15	86
IO19	17	87
IO2	19	88
IO18	21	89
IO1	23	90
NC13	25	91
IO0	27	92
NC12	29	95
IO49	31	96
Logic analyzer header connector P7		
NC11	1	97
IO48	3	98
NC10	5	99
NC7	7	100
NC9	9	101
NC6	11	102
NC8	13	103
NC5	15	104
MODRST~	17	105
NC4	19	106
BOOTMUX	21	107

Signal name	Logic analyzer header connector pin number	ConnectCore 9C pin number
NC3	23	108
IO16	25	109
NC2	27	110
IO17	29	111
NC1	31	112
Logic analyzer header connector P8		
OVR3 ~	1	113
OVR4 ~	3	114
PON3 ~	5	115
PON4 ~	7	116
OVR1 ~	9	117
OVR2 ~	11	118
PON1 ~	13	119
PON2 ~	15	120
DM4	17	123
DP4	19	124
DM3	21	127
DP3	23	128
DM2	25	131
DP2	27	132
DM1	29	135
DP1	31	136

I2C expander tables

I^{2}C expanders expand the number of GPIOs and add board ID. The ConnectCore 9C development board uses PCA9500 I^{2}C expanders. This expander has an internal 256 x 8 bit PCF8582C EEPROM. Three hardware pins — A0, A1, and A2 — vary the I^{2}C address and allow up to eight devices to share the same I^{2}C/SMBus. These devices are fully decoded on the development board.

The I/O expander's eight quasi-bidirectional data pins can be independently assigned as inputs or outputs to monitor board level status or activate indicator devices such as LEDs. The system master writes to the I/O configuration bits the data for each input or output. The system master can read all registers.

The EEPROM can store error codes or board manufacturing data for read-back by application software for diagnostic purposes, and is included in the I/O expander package. The PCA9500 appears as two separate devices to the bus master. The PCA9500 supports hot insertion to facilitate usage in removable cards on back-plane systems.

Following powerup, all eight I/Os default to input with a current source. There are no registers or latches on inputs. Reading a valid logic "0" requires a 1.0K pulldown to overcome this current source. Outputs have a data register and are open drain.

The next four tables show the breakdown of the I^{2}C expander. These are the I^{2}C default configurations.

I/O expander address 0

I/O	Expander Addr 0	Description
0	LED1	General purpose LED, CR28, 0 = ON
1	LED2	General purpose LED, CR18, 0 = ON
2	LED3	General purpose LED, CR10, 0 = ON
3	LED4	General purpose LED, CR8, 0 = ON
4	LED5	General purpose LED, CR27, 0 = ON
5	LED6	General purpose LED, CR17, 0 = ON
6	LED7	General purpose LED, CR9, 0 = ON
7	LED8/Write control	ALL expanders, I2C EEPROM LED, CR7, 0 = ON = Write enabled

Note: The LED8/Write control bit is connected to all four expanders' WE~ inputs. Setting this bit to a logic "0" enables writing to all four EEPROM.

I/O expander address 1

I/O	Expander Addr 1	Description
0	I2C_IO4 (VGA ID0)	MONITOR type ID bit 0, input from VGA connector p8.11 (optional)
1	SW2 ~	General purpose push button, SW9. Must be polled.
2	VGA_M1	VGA controller mode bit 1; set to output a 0.
3	VGA_M2	VGA controller mode bit 2; set to output a 0.
4	SD_WP	SD_MMC card write protect input, 0 = write protected.
5	I2C_IO9 (VGAID2)	MONITOR type ID bit 2, input from VGA connector P8.15 (optional)
6	SW1 ~	General purpose push button, SW1. Must be polled.
7	I2C_IO7 (VGA ID3)	MONITOR type ID bit 2, input from VGA connector P8.4 (optional)

Note: MONITOR type ID bit 1, input from VGA connector P8.12 is connected to I2C_DAT - GPIO[71] (optional).

I/O expander address 2

I/O	Expander Addr 2	Description
0	I2C_GPIO_0	General purpose I/O to P10.1
1	I2C_GPIO_1	General purpose I/O to P10.2
2	I2C_GPIO_2	General purpose I/O to P10.3
3	I2C_GPIO_3	General purpose I/O to P10.4
4	I2C_GPIO_4	General purpose I/O to P10.5
5	I2C_GPIO_5	General purpose I/O to P10.6
6	I2C_GPIO_6	General purpose I/O to P10.7
7	I2C_GPIO_7	General purpose I/O to P10.8

I/O expander address 3

I/O	Expander Addr 3	Description
0	I2C_GPIO_8	General purpose I/O to P10.9
1	I2C_GPIO_9	General purpose I/O to P10.10
2	I2C_GPIO_10	General purpose I/O to P10.11
3	I2C_GPIO_11	General purpose I/O to P10.12
4	I2C_GPIO_12	General purpose I/O to P10.13
5	I2C_GPIO_13	General purpose I/O to P10.14
6	I2C_GPIO_14	General purpose I/O to P10.15
7	I2C_GPIO_15	General purpose I/O to P10.16

GPIO channel descriptions

This section shows describes the different development board GPIO channels, detailing each signal path, NS9360-related function, and switch position.

Legend:

x	Position doesn't matter
N/C	No connection
Shaded	**This is the default setting**

The notes referred to are at the end of the table.

GPIO channel 0

		Switch position		
Signal path	NS9360 function	SW21-5	SW21-1	SW2-1
SPIB-DOUT to P14-2	SPI/B	on	x	x
TXDB to P23-3	UART/B	off	off	x
N/C	Localized	off	on	on
Connect to P1-1	GPIO	off	on	off

GPIO channel 1

		Switch position		
Signal path	NS9360 function	SW19-1	SW21-2	SW2-2
SPIB-DIN to P14-3	SPI/B	on	x	x
RXDB to P23-2	UART/B	off	off	x
N/C	Localized	off	on	on
Connect to P1-2	GPIO	off	on	off

GPIO channel 2

		Switch position	
Signal path	NS9360 function	SW21-3	SW2-3
RTSB to P23-7	UART/B	off	x
N/C	Localized	on	on
Connect to P1-3	GPIO	on	off

GPIO channel 3

		Switch position	
Signal path	NS9360 function	SW21-4	SW2-4
CTSB to P23-8	UART/B	off	x
N/C	Localized	on	on
Connect to P1-4	GPIO	on	off

GPIO channel 4

		Switch position
Signal path	NS9360 function	SW2-5
N/C	Localized	on
Connect to P1-5	GPIO	off

GPIO channel 5

		Switch position	
Signal path	NS9360 function	SW11-1	SW3-1
Control for LCD backlight	LCD/GPIO (see note 1)	off	x
N/C	Localized	on	on
Connect to P1-6	GPIO	on	off

GPIO channel 6

		Switch position	
Signal path	NS9360 function	SW11-2	SW3-2
SPICLKB to P14-4	SPI/B	off	x
N/C	Localized	on	on
Connect to P1-7	GPIO	on	off

GPIO channel 7

		Switch position	
Signal path	NS9360 function	SW11-3	SW3-3
Select for SPI (U22-4)	SPI/GPIO (see note 2)	off	x
N/C	Localized	on	on
Connect to P1-8	GPIO	on	off

GPIO channel 8

		Switch position	
Signal path	NS9360 function	SW19-2	SW3-4
TXDA to P22-3	UART/A	off	x
N/C	Localized	on	on
Connect to P1-9	GPIO	on	off

GPIO channel 9

		Switch position	
Signal path	NS9360 function	SW11-3	SW3-5
RXDA to P22-2	UART/A	off	x
N/C	Localized	on	on
Connect to P1-10	GPIO	on	off

GPIO channel 10

		Switch position	
Signal path	NS9360 function	SW19-4	SW4-1
RTSA to P22-7	UART/A	off	x
N/C	Localized	on	on
Connect to P2-1	GPIO/PWM0	on	off

GPIO channel 11

		Switch position		
Signal path	NS9360 function	SW 20-2	SW20-1	SW4-2
SD insertion/deinsertion	IRQ (see note 3)	on	x	x
CTSA to P22-8	UART/A	off	off	x
N/C	Localized	off	on	on
Connect to P2-2	GPIO	off	on	off

GPIO channel 12

		Switch position	
Signal path	NS9360 function	SW19-5	SW4-3
DTRA to P22-4	UART/A	off	x
N/C	Localized	on	on
Connect to P2-3	GPIO/PWM1	on	off

GPIO channel 13

		Switch position	
Signal path	NS9360 function	SW20-3	SW4-4
DSRA to P22-6	UART/A	off	x
N/C	Localized	on	on
Connect to P2-4	GPIO/PWM2	on	off

GPIO channel 14

		Switch position	
Signal path	NS9360 function	SW20-4	SW4-5
RIA to P22-9	UART/A	off	x
N/C	Localized	on	on
Connect to P2-5	GPIO/PWM3	on	off

GPIO channel 15

		Switch position	
Signal path	NS9360 function	SW20-5	SW5-1
DCDA to P22-1	UART/A	off	x
N/C	Localized	on	on
Connect to P2-6	GPIO	on	off

GPIO channel 23

		Switch position	
Signal path	NS9360 function	SW13-5	SW5-2
Control for LCD buffer	LCD/GPIO (see note 4)	off	x
N/C	Localized	on	on
Connect to P2-7	GPIO	on	off

GPIO channel 32

		Switch position	
Signal path	NS9360 function	SW12-1	SW5-3
LCD-D8 to buffer	LCD	off	x
N/C	Localized	on	on
Connect to P2-8	GPIO	on	off

GPIO channel 33

		Switch position	
Signal path	NS9360 function	Sw12-2	SW5-4
LCD-D9 to buffer	LCD	off	x
N/C	Localized	on	on
Connect to P2-9	GPIO	on	off

GPIO channel 34

		Switch position	
Signal path	NS9360 function	SW12-3	SW5-5
LCD-D10 to buffer	LCD	off	x
N/C	Localized	on	on
Connect to P2-10	GPIO	on	off

GPIO channel 35

		Switch position	
Signal path	NS9360 function	SW12-4	SW6-1
LCD-D11 to buffer	LCD	off	x
N/C	Localized	on	on
Connect to P3-1	GPIO	on	off

GPIO channel 36

		Switch position	
Signal path	NS9360 function	SW12-5	sw6-2
LCD-D12 to buffer	LCD	off	x
N/C	Localized	on	on
Connect to P3-2	GPIO/PWM0	on	off

GPIO channel 37

		Switch position	
Signal path	NS9360 function	13-1	SW6-3
LCD-D13	LCD	off	x
N/C	Localized	on	on
COnnect to P3-3	GPIO/PWM1	on	off

GPIO channel 38

		Switch position	
Signal path	NS9360 function	SW13-2	SW6-4
LCD-D14 to buffer	LCD	off	x
N/C	Localized	on	on
Connect to P3-4	GPIO/PWM2	on	off

GPIO channel 39

		Switch position	
Signal path	NS9360 function	Sw13-3	SW6-5
LCD-D15 to buffer	LCD	off	x
N/C	Localized	on	on
Connect to P3-5	GPIO/PWM3	on	off

GPIO channel 40

		Switch position
Signal path	NS9360 function	SW22-5
LCD-D16 to buffer	LCD	on
TXDC to P19-3	UART/C	off

GPIO channel 41

		Switch position
Signal path	NS9360 function	SW13-4
LCD-D17 to buffer	LCD	on
RXDC to P19-2	UART/C	off

GPIO channel 42

		Switch position		
Signal path	NS9360 function	SW22-3	SW22-1	SW7-1
USB DATA HI to PHY	USB Device	on	x	x
RTSC to P19-7	UART/C	off	off	x
N/C	Localized	off	on	on
Connect to P3-6	GPIO	off	on	off

GPIO channel 43

		Switch position		
Signal path	NS9360 function	SW22-4	SW22-2	SW7-2
USB DATA LO to PHY	USB Device	on	x	x
CTSC to P19-8	UART/C	off	off	x
N/C	Localized	off	on	on
Connect to P3-7	GPIO	off	on	off

GPIO channel 44

		Switch position		
Signal path	NS9360 function	SW17-5	SW17-4	SW7-3
USB OE LO to PHY	USB Device	on	x	x
TXDD to P15-3	UART/D	off	off	x
N/C	Localized	off	on	on
Connect to P3-8	GPIO	off	on	off

GPIO channel 45

		Switch position		
Signal path	NS9360 function	SW17-1	SW17-2	SW7-4
USB RCV to PHY	USB Device	on	x	x
RXDD to P15-2	UART/D	off	off	x
N/C	Localized	off	on	on
Connect to P3-9	GPIO	off	on	off

PIO channel 46

		Switch position		
Signal path	NS9360 function	SW15-2	SW15-1	SW7-5
USB ENUM to PHY	USB Device	on	x	x
RTSD to P15-7	UART/D	off	off	x
N/C	Localized	off	on	on
Connect to P3-10	GPIO	off	on	off

GPIO channel 47

		Switch position	
Signal path	NS9360 function	SW17-3	SW8-1
CTSD to P15-8	UART/D	off	x
N/C	Localized	on	on
Connect to P5-1	GPIO	on	off

GPIO channel 48

		Switch position	
Signal path	NS9360 function	SW11-4	SW8-2
USB SUSPEND to PHY	USB Device	off	x
N/C	Localized	on	on
Connect to P5-2	GPIO/PWM3	on	off

GPIO channel 49

		Switch position	
Signal path	NS9360 function	Sw11-5	SW8-3
USB SPEED to PHY	USB Device	off	x
N/C	Localized	on	on
Connect to P5-3	GPIO	on	off

Table notes

1 The LCD backlight requires the signal to be set up as a GPIO output. LCD backlight is enabled on logic 0.

2 SPI device selection for encoder. this requires the signal to be set up as a GPIO output. See U22 (in the schematics on your CD) for details.

3 Used as an IRQ input to find the presence of an SD/MMC card.

4 LCD buffer enable requires this signal to be set up as a GPIO output and driven logic 0.

Factory default interface configuration for development board

These interfaces are enabled as shown per the factory default configuration:

Interface	Factory default status
LCD interface	Enabled
LCD VGA	Enabled
LCD backlight	Enabled
I^2C (5V tolerant)	Enabled
I^2C user-driven LEDs	Enabled
USB Device	Enabled
USB Host	Enabled
EIA-232-Serial Port A (full modem support)	Enabled

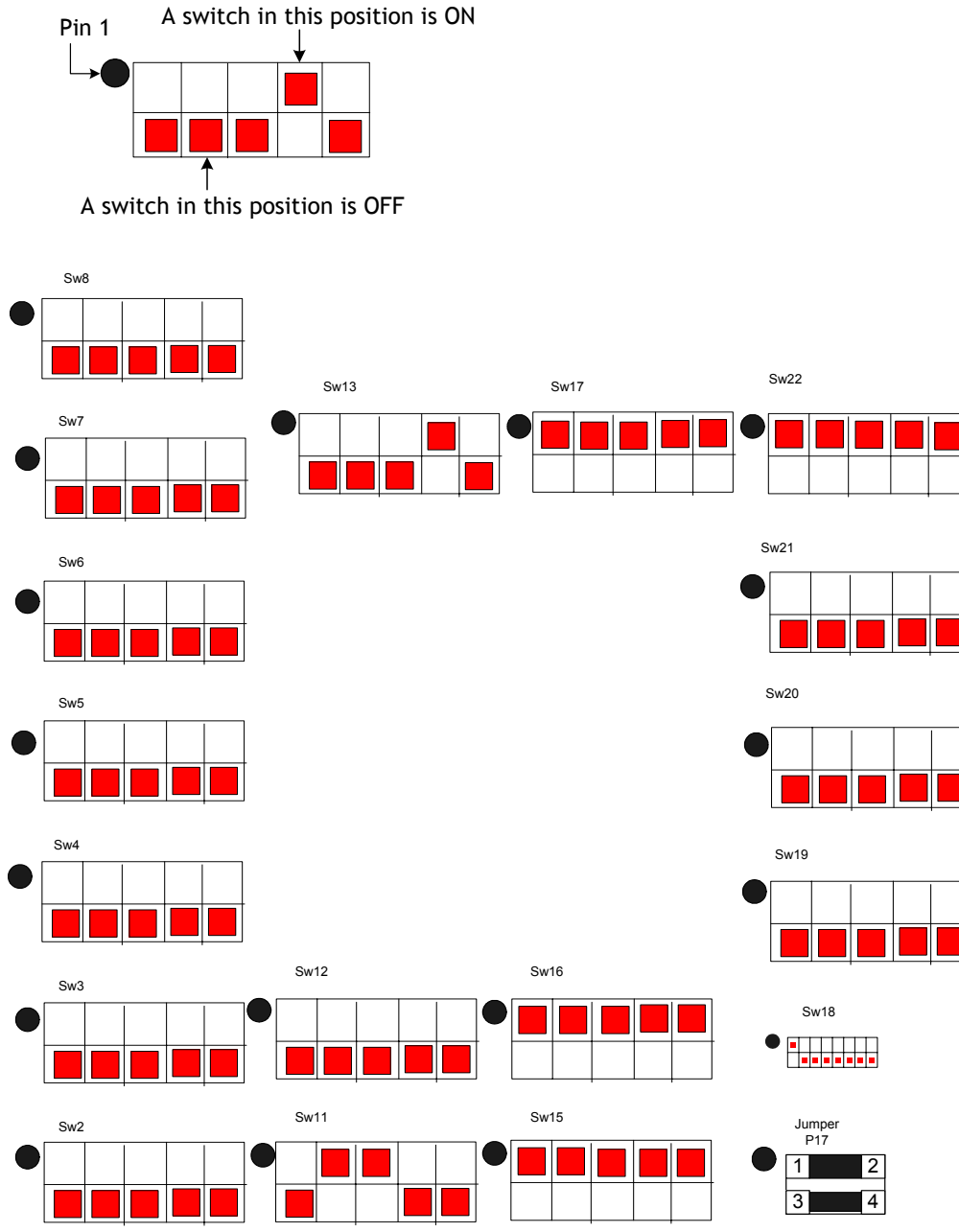
Interface	Factory default status
EIA-232-Serial Port B	Enabled
EIA-232-Serial Port C	Disabled
EIA-232-Serial Port D	Disabled
EIA-485-Serial Port A	Disabled
SPI	Disabled
Touch screen	Disabled
MMC/SD socket	Disabled

GPIO#	Factory default status
GPIO_4	Enabled
GPIO_6	Enabled
GPIO_7	Enabled
GPIO_47	Enabled
I^2C GPIO[0:15]	Enabled

USB hub	Default status assumption
On module	Not present
On development board	Present

Default switch configurations

- The black dot next to each switch indicates pin 1.
- Switch positions:


Pin 1
A switch in this position is ON
A switch in this position is OFF
Sw8
Sw7
Sw6
Sw5
Sw4
Sw3
Sw2
Sw13
Sw17
Sw22
Sw21
Sw20
Sw19
Sw12
Sw16
Sw18
Sw11
Sw15
Jumper
P17
1
2
3
4

Jumper 17 signal table

DR1R (pin 1)	Short to (default)	USB_H_DM (pin 2)	Select HUB on development boards
DP1R (pin 3)	Short to (default)	USB_H_DP (pin 4)	
DM1R (pin 1)	Open with	USB_H_DM (pin 2)	Select HUB on module
DP1R (pin 3)	Open with	USB_H_DP (pin 4)	

Note: When selecting the USB hub on either the development board or the module, modify SW15 and SW16 appropriately.

Development board LEDs

The development board has seven sets of LEDs:

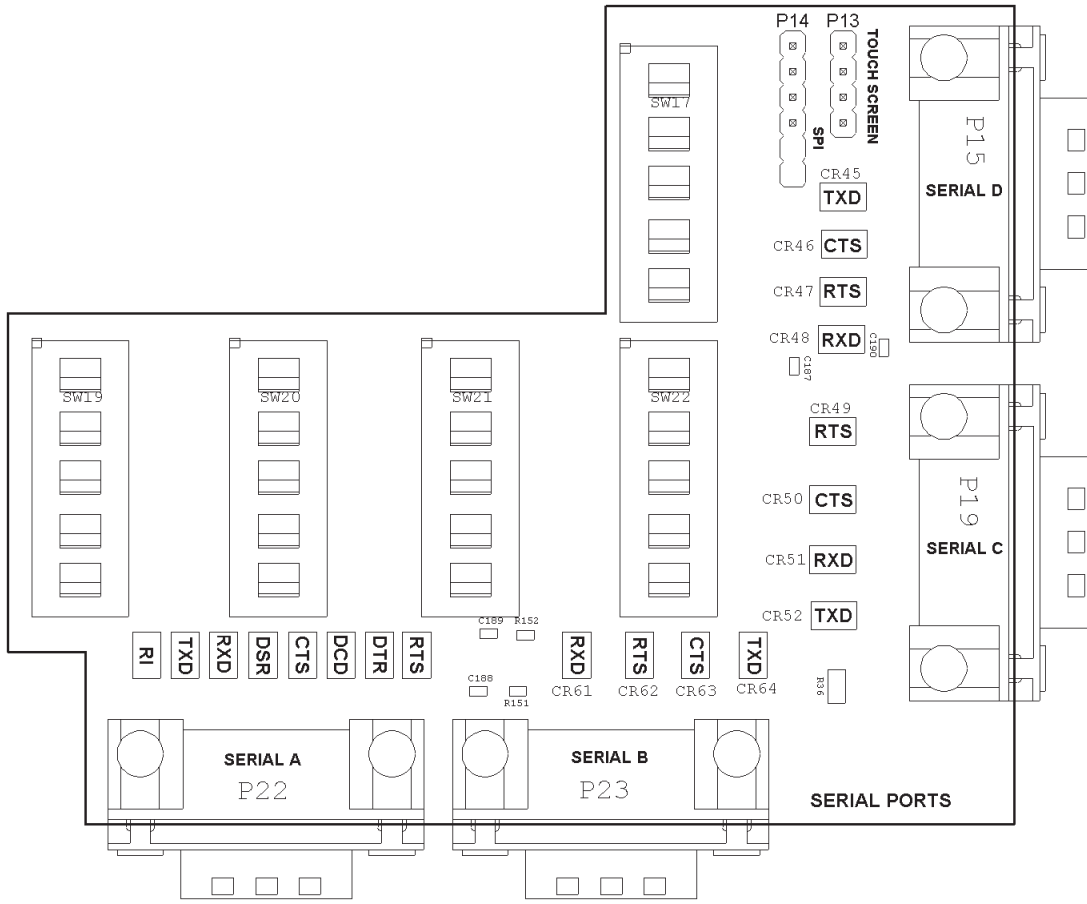
1. Serial port A, EIA-232
2. Serial port A, EIA-485
3. Serial ports B, C, and D, EIA-232
4. Power and I^2C
5. GPIO bank connector (terminal strip) P1
6. GPIO bank connector P2
7. GPIO bank connector P3 and additional GPIO bank P5

Each set of LEDs is described in the following sections.

1-3: Serial Ports

LED locations

The LEDs are above serial ports A and B, and to the left of serial ports C and D.



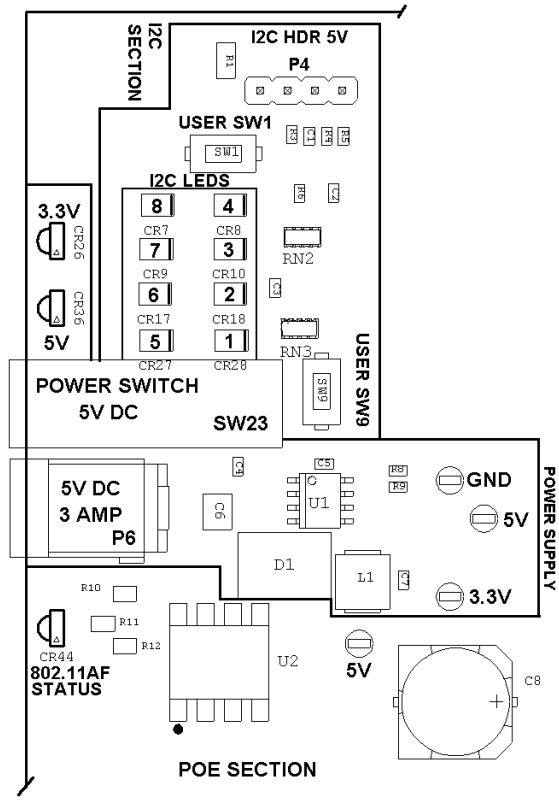
The LED indicators are dual state, and are connected to the UART side of the EIA transceivers.

- Green represents a negative voltage on the DB9 connector pin.
- Red represents a positive voltage on the DB9 connector pin.

The intensity and color of the LED will change when the voltage is switching.

4: Power and I²C

LED locations



Power and I²C description

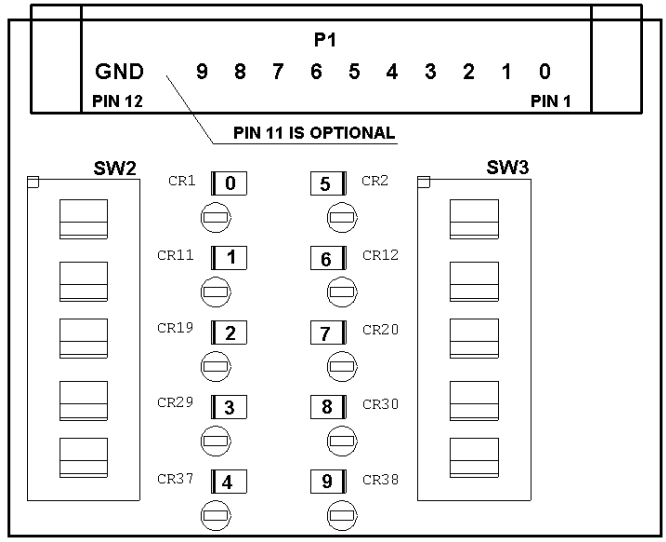
LED	Condition when green	Source
5V, CR36	5V power is present	P6 power jack or PoE (optional)
3.3V, CR26	3.3V power is present	U1 DC/DC regulator
802.3af, CR44	PoE power present	LAN connector on module
I2C-1, CR28	I2C Expanded Addr0, bit 0 = 0	U10.4
I2C-2, CR28	I2C Expanded Addr0, bit 1 = 0	U10.5

LED	Condition when green	Source
I2C-3, CR10	I2C Expanded Addr0, bit 2 = 0	U10.6
I2C-4, CR8	I2C Expanded Addr0, bit 3 = 0	U10.7
I2C-5, CR27	I2C Expanded Addr0, bit 4 = 0	U10.9
I2C-6, CR17	I2C Expanded Addr0, bit 5 = 0	U10.10
I2C-7, CR9	I2C Expanded Addr0, bit 6 = 0	U10.11
I2C-8, CR7	I2C Expanded Addr0, bit 7 = 0	U10.12

5: GPIO terminal strip P1

LED locations

Note: Bold numbers on the figure represent actual GPIO numbers.



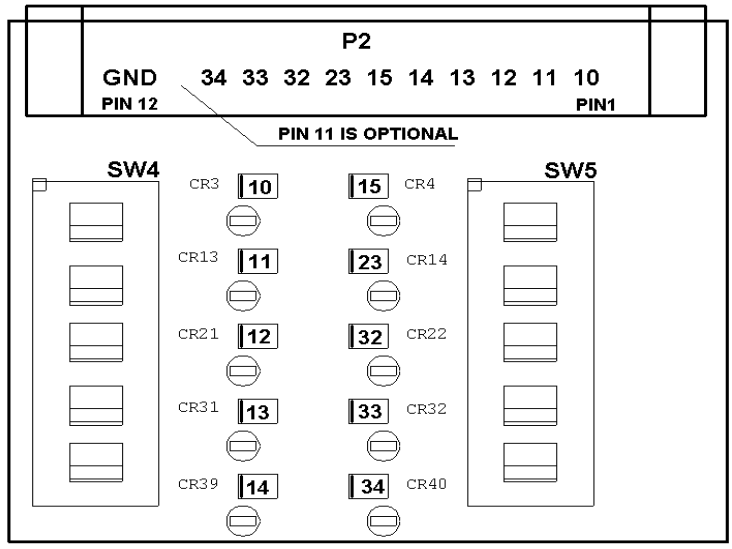
GPIO terminal strip P1 descriptions

Green LED, SO-DIMM pin #	Condition when Off	Source
IO1, 90	GPIO[0] = 0 or SW2.1 = ON	U8.18
IO2, 77	GPIO[1] = 0 or SW2.2 = ON	U8.16
IO3, 86	GPIO[2] = 0 or SW2.3 = ON	U8.14
IO4, 84	GPIO[3] = 0 or SW2.4 = ON	U8.12
IO5, 80	GPIO[4] = 0 or SW2.5 = ON	U8.9
IO6, 78	GPIO[5] = 0 or SW3.1 = ON	U8.7
IO7, 76	GPIO[6] = 0 or SW3.2 = ON	U8.5
IO8, 85	GPIO[7] = 0 or SW3.3 = ON	U8.3
IO9, 83	GPIO[8] = 0 or SW3.4 = ON	U7.18
IO10, 79	GPIO[9] = 0 or SW3.5 = ON	U7.16

6: GPIO terminal strip P2

LED locations

Note: Bold numbers on the figure represent actual GPIO numbers.



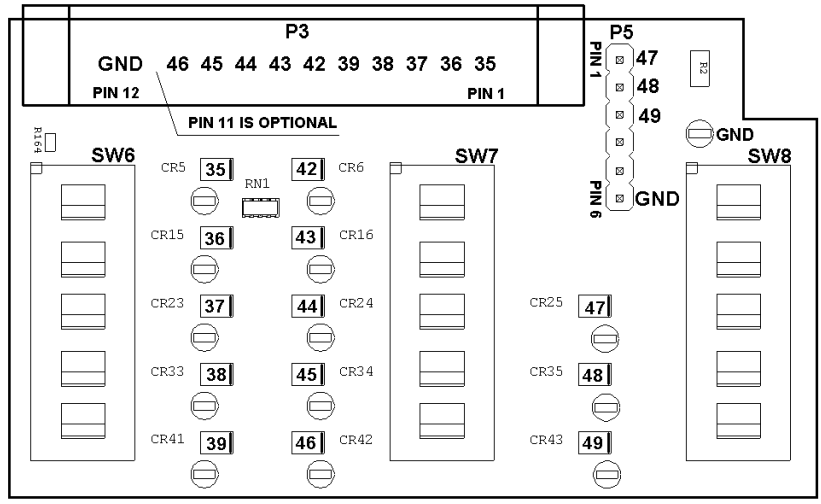
GPIO terminal strip P2 descriptions

Green LED	Condition when Off	Source
IO11, 77	GPIO[10] = 0 or SW4.1 = ON	U7.14
IO12, 75	GPIO[11] = 0 or SW4.2 = ON	U7.12
IO13, 73	GPIO[12] = 0 or SW4.3 = ON	U7.9
IO14, 69	GPIO[13] = 0 or SW4.4 = ON	U7.7
IO15, 67	GPIO[14] = 0 or SW4.5 = ON	U7.5
IO16, 109	GPIO[15] = 0 or SW5.1 = ON	U7.3
IO17, 111	GPIO[23] = 0 or SW5.2 = ON	U6.18
IO18, 89	GPIO[32] = 0 or SW5.3 = ON	U6.16
IO19, 87	GPIO[33] = 0 or SW5.4 = ON	U6.14
IO20, 46	GPIO[34] = 0 or SW5.5 = ON	U6.12

7: GPIO terminal strips P3 and P5

LED locations

Note: Bold numbers on the figure represent actual GPIO numbers.



GPIO terminal strip P3 and P5 descriptions

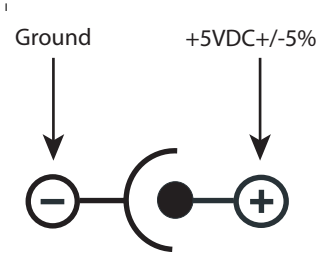
Green LED	Condition when Off	Source
IO21, 44	GPIO[35] = 0 or SW6.1 = ON	U6.9
IO22, 42	GPIO[36] = 0 or SW6.2 = ON	U6.7
IO23, 38	GPIO[37] = 0 or SW6.3 = ON	U6.5
IO24, 37	GPIO[38] = 0 or SW6.4 = ON	U6.3
IO25, 35	GPIO[39] = 0 or SW6.5 = ON	U5.18
IO26, 33	GPIO[42] = 0 or SW7.1 = ON	U5.16
IO27, 31	GPIO[43] = 0 or SW7.2 = ON	U5.14
IO28, 65	GPIO[44] = 0 or SW7.3 = ON	U5.12
IO29, 74	GPIO[45] = 0 or SW7.4 = ON	U5.9
IO30, 63	GPIO[46] = 0 or SW7.5 = ON	U5.7
IO31, 70	GPIO[47] = 0 or SW8.1 = ON	U5.5
IO32, 57	GPIO[48] = 0 or SW8.2 = ON	U5.3
IO33, 68	GPIO[49] = 0 or SW8.3 = ON	U11.18

Power jack

The power jack is a barrel connector that accepts +5VDC ± 5%. The jack is labeled as P6 on the development board. This table shows the power jack's polarity.

Contact	Polarity
Center	+ 5VDC ± 5%
Outer	Ground

This figure schematically represents the power jack's polarity.



Power switch, SW23

Power switch SW23 is the main power switch. Putting the lever in the down position turns off the power.

Test points

The development board provides 47 test points that can be identified by board label or test point number. The board labels are adjacent to each test point on the board. The test point numbers are in the development board schematic drawings. This table lists the test point number and description.

Test point	Description	Test point	Description
TP1	Ground	TP25	GPIO-38
TP2	GPIO-0	TP26	GPIO-45
TP3	GPIO-5	TP27	GPIO-48
TP4	GPIO-10	TP28	+ 5v
TP5	GPIO-15	TP29	GPIO-4
TP6	GPIO-35	TP30	GPIO-9
TP7	GPIO-42	TP31	GPIO-14
TP8	GPIO-1	TP32	GPIO-34
TP9	GPIO-6	TP33	GPIO-39
TP10	GPIO-11	TP34	GPIO-46
TP11	GPIO23	TP35	GPIO-49
T12	GPIO-36	TP36	GND
TP13	GPIO-43	TP37	+ 3.3V
TP14	GPIO-2	TP38	+ 5V
TP15	GPIO-7	TP39	GND
TP16	GPIO-12	TP40	PoE_GND
TP17	GPIO-32	TP41	GND
TP18	GPIO-37	TP42	GND
TP19	GPIO-44	TP43	GND
TP20	GPIO-47	TP44	POETCT
TP21	GPIO-3	TP45	POERCT
TP22	GPIO-8	TP46	POEA

Test point	Description	Test point	Description
TP23	GPIO-13	TP47	POEB
TP24	GPIO-33		

LCD and USB Considerations

CHAPTER 3

This chapter addresses ConnectCore 9C specifics pertaining to the LCD and USB interfaces.

See the application note “LCD Displays Supported by the NetSilicon NS9750/NS9360 Processors” for additional information about the application-specific configuration and capabilities of the LCD controller on the ConnectCore 9C module. This application note is available in the Support section of the Digi and NetSilicon web site.

LCD displays

There are seven categories of LCD displays, all of which the ConnectCore 9C supports:

- Color TFT (*thin film transistor*, also called *active matrix* (AM)):
  - 18-bit
- Six types of STN (*super twisted nematic*, also called *passive matrix* (PM)):
  - Three single panel displays
  - Three dual panel displays

Each STN display is either color or monochrome:

- Color display: Up to 8-pin using color-enhancing palette RAM
- Monochrome display: Up to 8-pin or 4-pin using grayscale-enhancing palette RAM

Control and data pins

The ConnectCore 9C LCD interface has six control pins. The number of data pins depends on the display type. Displays typically require 4–6 control pins. The next two tables list the control pins and the data pins, respectively.

LCD controller control pins

Signal name	Type	Description
CLPOWER	Output	LCD panel power enable
CLLP	Output	Line synchronization pulse (STN)/horizontal synchronization pulse (TFT)
CLCP	Output	LCD panel clock
CLFP	Output	Frame pulse (STN)/vertical synchronization pulse (TFT)
CLAC	Output	STN AC bias drive or TFT data enable output
CLLE	Output	Line end signal

LCD controller data pins

Display type	Number of data pins: Panel 1	Number of data pins: Panel 2
TFT—Color only		
Color 18-bit	18	Not applicable
STN—Color		
Single panel 8-bit	8	Not applicable
Dual panel 8-bit	8	8
STN—Monochrome		
Single panel 4-bit	4	Not applicable
Dual panel 4-bit	4	4
Single panel 8-bit	8	Not applicable
Dual panel 8-bit	8	8

Note: Double-panel displays use twice as many pins but do not offer more color or gray shades.

Colors and gray shades

The number of colors and gray shades correlates with the number of data pins but also depends on color processing techniques and data-shifting techniques. (For exact values, see the *NS9360 Hardware Reference*, P/N: 90000675_A, at *www.netsilicon.com/support/ns9360userguides.jsp*, LCD Controller chapter, and search on *Number of colors* and *Grayscaler*).

ConnectCore 9C uses an internal programmable palette-LUT and a grayscaler to support different color-processing techniques; three sample displays are provided here:

- **18-pin TFT display** (for example, the SHARP LQ10D421). Accepts 18 color RGB bits (6 bits per color) at a time. Only 16 bits are transferred from SDRAM: five bits each for the three colors — R (red), G (green), and B (blue) — and a single LSB (least significant bit) that is split into three equal values between R, G, and B. This produces close to 2^{16}, or 64 thousand colors.
- **8-pin STN color display** (for example, the SHARP LM057QC1T01). Shifts eight color bits at a time: RGBRGBRG bits followed by BRGBRGBR bits followed by GBRGBRGB, and so on. This produces color enhancing in 3375 color grades.
- **4-pin STN monochrome display** (for example, the Grand Pacific Optoelectronics GM0008-13). Shifts four monochrome bits at a time, resulting in 15 gray shades ($2^4 - 1$).

Resolution

The LCD resolution is programmable. These standard displays, with the following resolutions, are supported:

- QVGA = 320 x 240
- VGA = 640 x 480
- SVGA = 800 x 600

Lower resolution displays also are supported. Displays typically have programmable vertical resolutions within a certain range, especially if they are used for TV displays (to accommodate different television standards).

Refresh frequency

The LCD refresh frequency is programmable. Lower refresh frequency drains less power, but might flicker. For that reason, laptop screens refresh at higher rates. TV sets may require a refresh of 50Hz (SECAM, PAL, used in Europe) or 60Hz (NTSC, used in the United States). TFT displays usually flicker less than STN displays, as they have a transistor switch behind each pixel on the screen and can hold the capacitive charge longer.

Sample applications

To reduce the system cost, the LCD interface uses memory as a video buffer. The display resolution is determined by the product of three parameters: *number of data bits x display resolution x refresh frequency.* This product cannot exceed the system bus bandwidth allocated to the display.

The ConnectCore 9C module operates in conjunction with the NS9360's industrial temperature range (-40º to 85º) with an operating speed of 155 MHz.

Formula

The ConnectCore 9C module operates at 155 MHz system bus speed. This speed grade results in 310 Mbps bus bandwidth, as the bus is 4 bytes wide. For bandwidth planning, this maximum bandwidth must be reduced to account for overhead and read/write switching. The effective bandwidth is 1/2 of the system bandwidth; that is, 155 Mbps. This value is predicted as the worst case for the ConnectCore 9C. The architecture allocates half of the system bandwidth to the module. The remaining four bus master peripherals (Ethernet TX, Ethernet RX, peripheral bus bridge, and LCD controller) share the other half of the bandwidth. The bandwidth assignment of these peripherals is programmable.

Use this formula to estimate the amount of bandwidth available for your LCD display:

```
Module bandwidth = 77.5 Mbps
All other peripherals (including LCD) = 77.5 Mbps
```

Example 1: 18-bit VGA

The 18-bit TFT display transfers 16 bits per pixel and generates the last two bits inside the LCD controller. This display packs two-color RGB pixels into a single 4-byte word.

The 18-bit VGA display (640 x 480), refreshing 60 times per second, requires 37 MBps:

```
2 x 640 x 480 x 60 = 37 MBps
```

40.5 MBps are left to all other peripherals. If the LCD refresh frequency increases to 70 Hz, the required bandwidth increases to 43 MBps.

Note: The module LCD controller supports 18-bit VGA displays in most applications.

Example 2: 18-bit SGA

The 18-bit SGA display with 60 MHz refresh requires 58 MBps:

```
2 x 800 x 600 x 60 = 58 MBps
```

19.5 MBps are left to other peripherals. If your application transfers a new image of this size (that is, 2 x 1024 x 768 = 1.6MB) over 100bT Ethernet in one direction less often than once per second, this display can be supported in your application (see "Supported TFT displays"). Lowering the refresh frequency to 50 HZ drops the LCD bandwidth requirement to 48 MBps.

Note: The module LCD controller can support 18-bit SGA displays in many applications.

Supported TFT displays

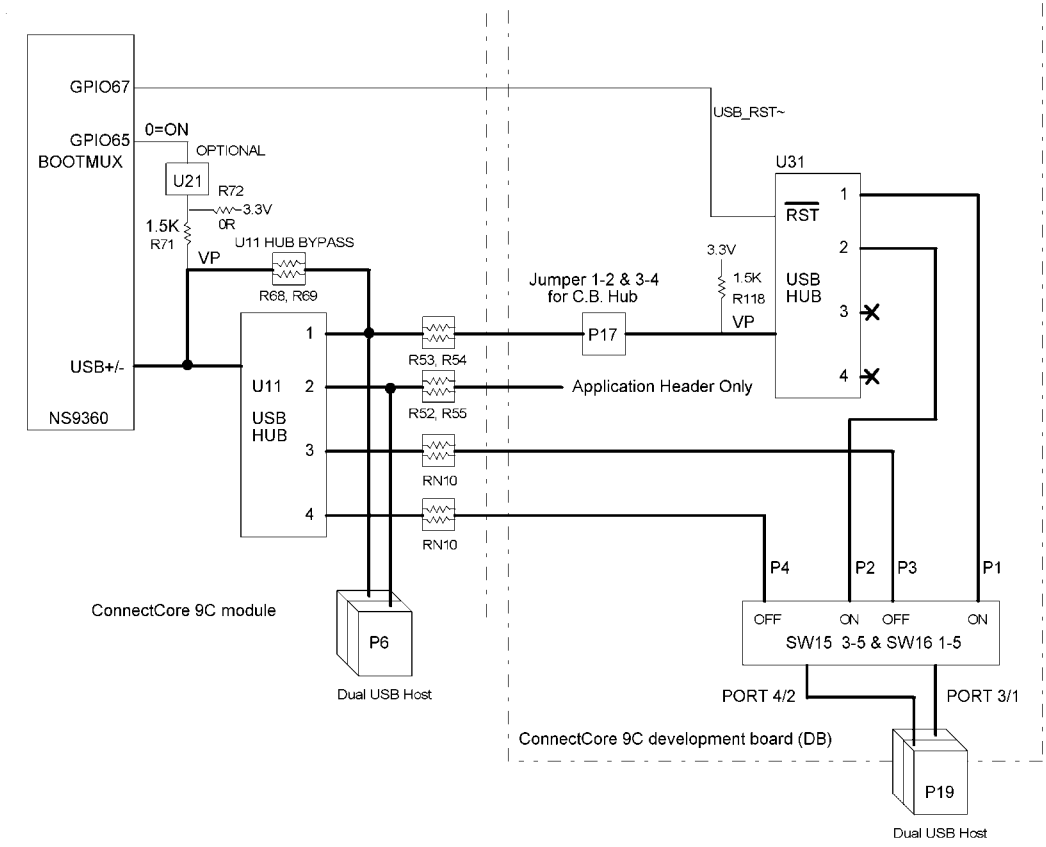
Display type	Refresh frequency in Hz	BW required for display in MBps	BW left to other peripherals in MBps
18b VGA (640 x 480)	50	31	46.5
	60	37	40.5
	70	43	34.5
18b SGA (800 x 600)	50	48	29.5
	60	58	19.5
	70	68	9.5

USB configuration

There are two USB configurations. See the USB configuration illustration for the exact location of each USB hub.

- The USB hub is on the module. When you purchase the Ethernet plus USB hub version of the ConnectCore 9C module, the USB hub is installed on the module at location U11.
- The USB hub is on the development board. When you purchase a development kit, the USB hub/device support is provided on the development board only, at location U31.

  USB Device is an external PHY, located at U38, and is wired directly to the NS9360 chip.



USB hub on the module (U11)

When configuring the USB hub on the ConnectCore 9C module, host ports 1 and 2 are connected to the module USB connector: P6, (Port 1 = lower). Host ports 3 and 4 are connected to the development board USB connector: P20, (Port 3 = lower).

Development board

- P17 No jumpers
- Switches:

Switch	Subswitch	Setting
SW15	3–5	OFF
SW16	1–5	OFF

USB hub on the development board (U31, default)

When configuring the USB hub on the development board, Host ports 1 and 2 are connected to the development board USB connector: P20, (Port 1 = lower). Host ports 3 and 4 are not connected.

Development board

- P17 Jumper 1-2, 3-4
- Switches:

Switch	Subswitch	Setting
SW15	3–5	ON
SW16	1–5	ON

See "USB internal PHY DC electrical inputs and outputs" on page 106 for information about integrating the module without on-board USB and without need for USB.

ConnectCore 9C Module Specifications

APPENDIX A

This appendix provides specifics about the ConnectCore 9C module.

Mechanical dimensions

- Length: 3.5 inches (88.9 mm)
- Width: 2.1 inches (53.34 mm)
- Height: 0.8 inches (20.32 mm) with RJ-45 Ethernet connector

Environmental information

- Operating temperature: -40° C to +85° C (-40° F to +185° F)
- Storage temperature: -40° to +125°
- Relative humidity: 5% to 95% (non-condensing)
- Altitude: 12,000 ft (3657.6 m)

Network interface

- Standard: IEEE 802.3
- Physical layer: 10/100Base-T
- Data rate: 10/100 Mbps (auto-sensing)
- Mode: Full or half duplex (auto-sensing)
- On-board connector: RJ-45 with magnetics
- 802.3af power pass-through (mid-span and end-span)

Power requirements

- Module: 3.3VDC @ 750 mA max
- USB interface: 5VDC @ 500mA max per port (optional)

Power up

The rise time of 3.3V power supply must be between 700 μA and 140 ms, and the inrush current must be limited to less than 2A.

Internal DC power sources

- 3.3V@360mA typical and 450mA max for NS9360, memory, logic, LEDs, and physical layer device (PHY)
- 5V@1A, for USB devices connected to the module with on-board USB support

I^2C signal muxing

The I^2C signals are muxed behind GPIO, as noted in the *Signal name / muxed behind* column.

Legend:

- SO-DIMM pin #: Pin number assignment for signal
- Signal: Pin name for each signal.
- U/D: Indicates whether the pin has an internal pullup resistor (U) or a pulldown resistor (D). If no value appears in the column, that pin has neither an internal pullup nor pulldown resistor.
- I/O: Type of signal input (I), output (O), or input/output (I/O)
- OD (mA): The output drive of an output buffer.

SO-DIMM Pin#	Signal name / muxed behind	U/D	OD (mA)	I/O	Description
55	iic_scl / gpio[34]		4	I/O	I^2C serial clock line. Add a 10K resistor to VDDA(3.3V) if used.
66	iic_sda / gpio[35]		4	I/O	I^2C serial data line. Add a 10K resistor to VDDA(3.3V) if used.

USB interface signals

If you are not using the USB interface on a module without on-board USB Host support, the pins noted in this table should be pulled down to ground through a 15K ohm resistor.

Note: All output drivers for USB meet the standard USB driver specifications.

Legend:

- SO-DIMM in #: Pin number assignment for signal
- Signal: Pin name for each signal.
- I/O: Type of signal input (I), output (O), or input/output (I/O)

SO-DIMM Pin #	Signal name / muxed behind	I/O	Description
135	usb_dm	I/O	USB data -
136	usb_dp	I/O	USB data +

Module reset

- Active low signal (MODRST~).
- An ADM811S voltage supervisor is provided to reset the ConnectCore 9C module at any time the power phases out. If +3.3V power supply dips below 2.93 volts, the ADM811S asserts and holds the reset signal.

  The ADM811S asserts the hard reset signal, causing the entire system to go into reset. Manual reset input is wired to ADM811S from JTAG header P2.
- The minimum pulse width for reset signal is 10μs.

Cabling

You can use two different cables with the ConnectCore 9C module:

- Standard CAT5 Ethernet cable
- USB Host type A cable

Electrical characteristics

The ConnectCore 9C operates at a 1.5V core, with 3.3V I/O ring voltages.

Absolute maximum ratings

Permanent device damage can occur if the absolute maximum ratings are ever exceeded.

Parameter	Symbol†	Rating	Unit
DC supply voltage	V_{DDA}	-0.3 to +3.6	V
DC input voltage	V_{INA}	-0.3 to V_{DDA} + 0.3	V
DC output voltage	V_{OUTA}	-0.3 to V_{DDA} + 0.3	V
DC input current	I_{IN}	±10	mA
Storage temperature	T_{STG}	-40 to +125	^{o}C
† V_{DDA}, V_{INA}, V_{OUTA}: Ratings of I/O cells for 3.3V interface			

Recommended operating conditions

Recommended operating conditions specify voltage and temperature ranges over which a circuit's correct logic function is guaranteed. The specified DC electrical characteristics (see "DC electrical characteristics," beginning on page 105) are satisfied over these ranges.

Parameter	Symbol†	Rating	Unit
DC supply voltage	V_{DDA}	3.0 to 3.6	V
	V_{DDC} (core) V_{DDC} (PLL)	1.4 to 1.6 1.425 to 1.575	V
Maximum junction temperature	T_J	125	^{o}C

† V_{DDA}: Ratings of I/O cells for 3.3V interface
V_{DDC}: Ratings of internal cells

Power dissipation

The *typical power dissipation* for the module is 1.6W.

DC electrical characteristics

DC characteristics specify the worst-case DC electrical performance of the I/O buffers that are guaranteed over the specified temperature range.

Inputs and outputs

Inputs

All electrical inputs are 3.3V interface.

Note: V_{SS} = 0V (GND)

Sym	Parameter	Condition	Value		Unit
V_{IH}	High-level input voltage: LVTTL level		Min	 2.0	 V
V_{IL}	Low-level input voltage: LVTTL level		Max	 0.8	 V
I_{IH}	High level input current (no pulldown)	$V_{INA} = V_{DDA}$	Min/Max	-10/10	µA
	Input buffer with pulldown		Min/Max	10/200	µA
I_{IL}	Low-level input current (no pullup	$V_{INA} = V_{SS}$	Min/Max	-10/10	µA
	Input buffer with pullup		Min/Max	10/200	µA
I_{OZ}	High-impedance leakage current	$V_{OUTA} = V_{DDA}$ or V_{SS}	Min/Max	-10/10	µA
I_{DDS}	Quiescent supply current	$V_{INA} = V_{DDA}$ or V_{SS}	Max	TBD	

Outputs

All electrical outputs are 3.3V interface.

Sym	Parameter	Value		Unit
V_{OH}	High-level output voltage (LVTTL)	Min	V_{DDA}-0.6	V
V_{OL}	Low-level output voltage (LVTTL)	Max	0.4	V

USB internal PHY DC electrical inputs and outputs

The development board provides USB Host and Device connectors; the ConnectCore 9C module optionally provides a USB Host port. The USB internal PHY DC electrical inputs and outputs are used only when there is no USB configuration on the module.

USB internal PHY DC electrical inputs

Symbol	Parameter	Min	Max	Units	Notes
V_{IH}	Input high level (driven)	2.0		V	
V_{IZ}	Input high level (floating)	2.7	3.6	V	
V_{IL}	Input low level		0.8	V	
V_{DI}	Differential input sensitivity	0.2		V	1
V_{CM}	Differential common mode range	0.8	2.5	V	2

Notes:

1 |(usb_dp) – (usb_dm)|

2 Includes V_{DI} range.

USB internal PHY DC electrical outputs

Symbol	Parameter	Min	Max	Units	Notes
V_{OL}	Output low level	0.0	0.3	V	1
V_{OH}	Output high level	2.8	3.6	V	2
V_{CRS}	Output signal crossover voltage	1.3	2.0	V	3

Notes:

1 Measured with R_L of 1.425k ohm to 3.6V.

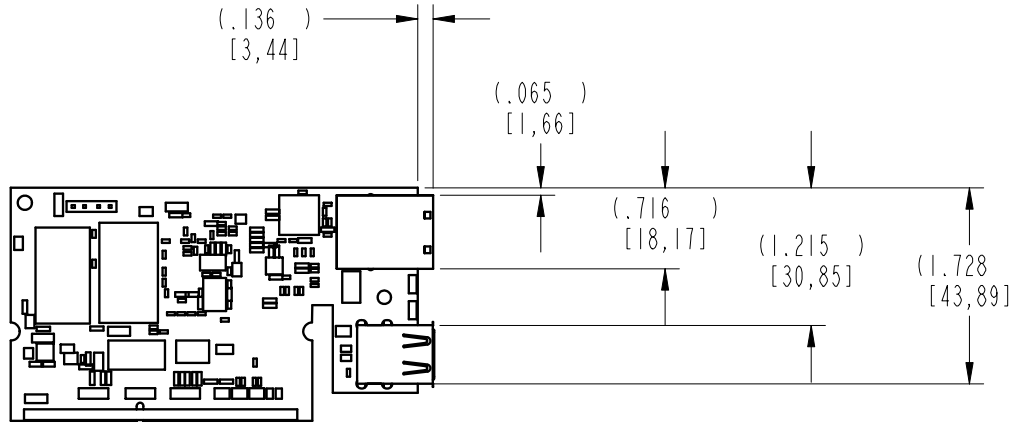
2 Measured with R_L of 14.25k ohm to GND.

3 Excluding the first transition from the idle state.

ConnectCore 9C module dimensions

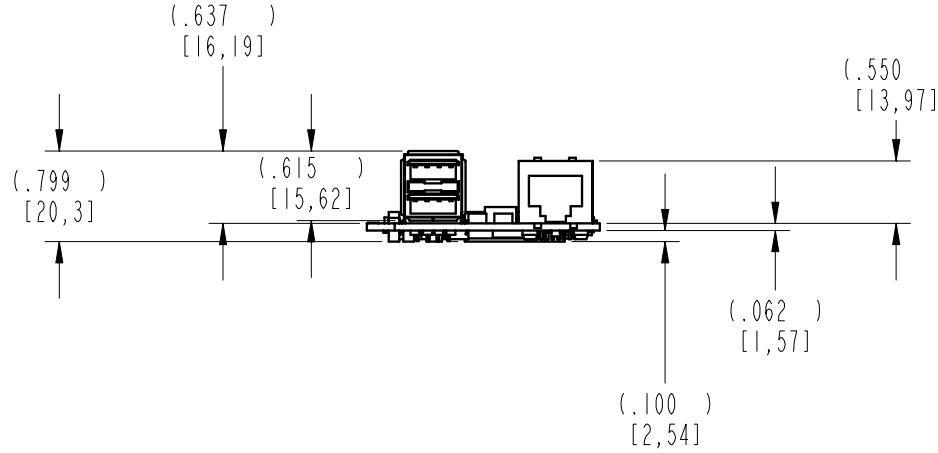
The next figures show the dimensions of the ConnectCore 9C module. Dimensions are in inches.

Top view

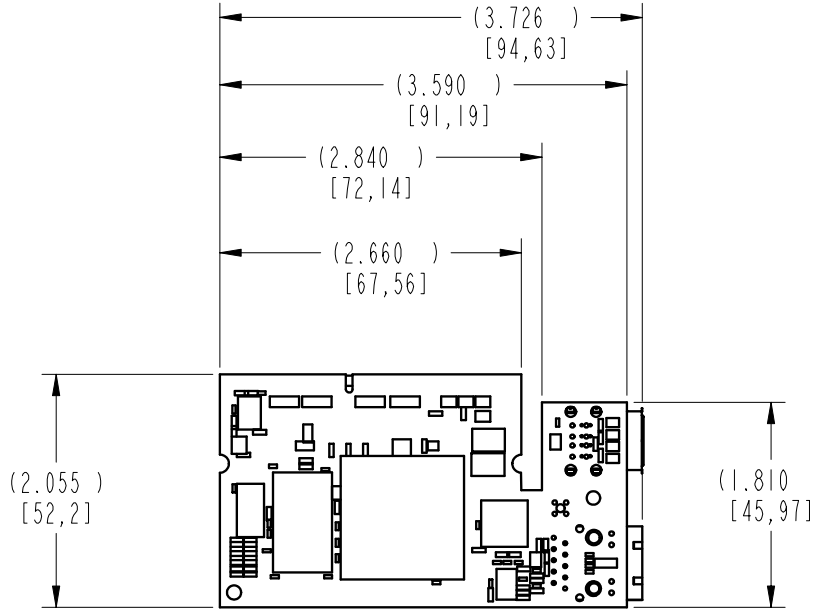


Side view

End view



Bottom view

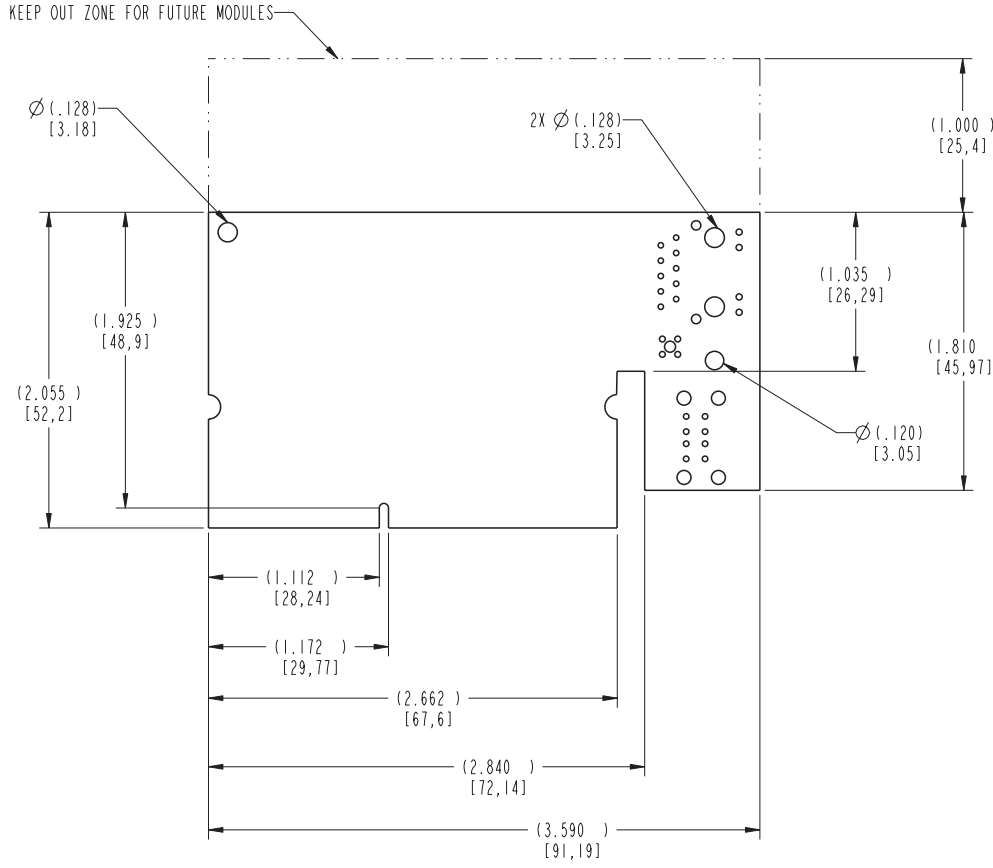


PCB layout

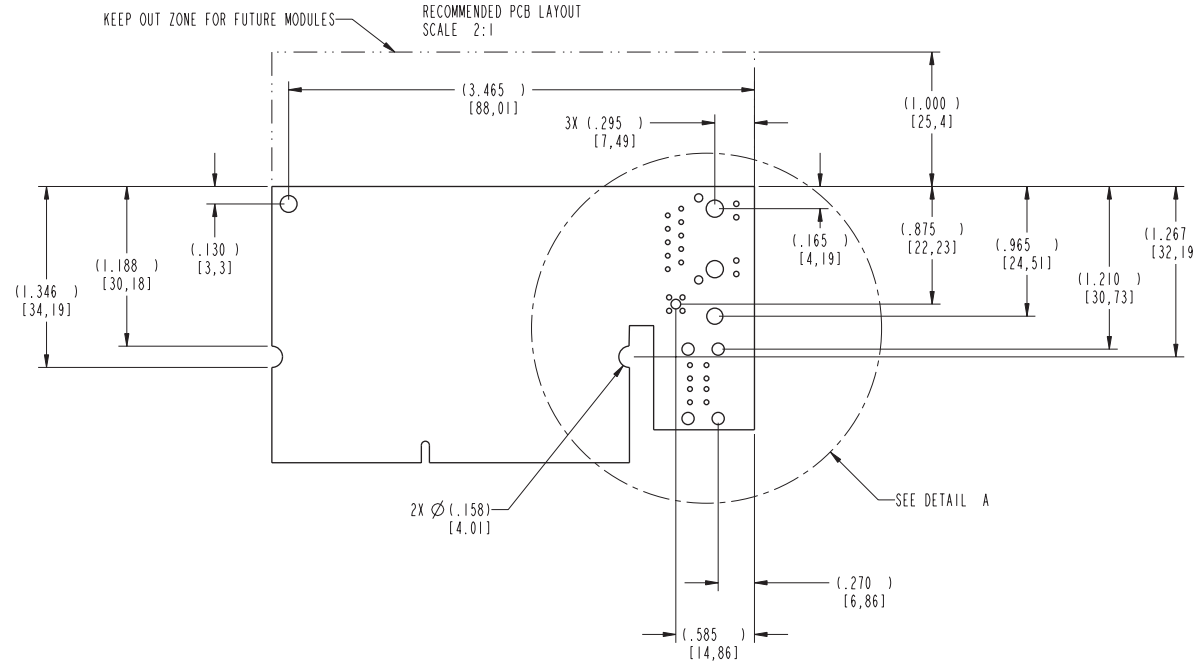
The next figures show the PCB (printed circuit board) layout of the ConnectCore 9C module:

Overall dimensions

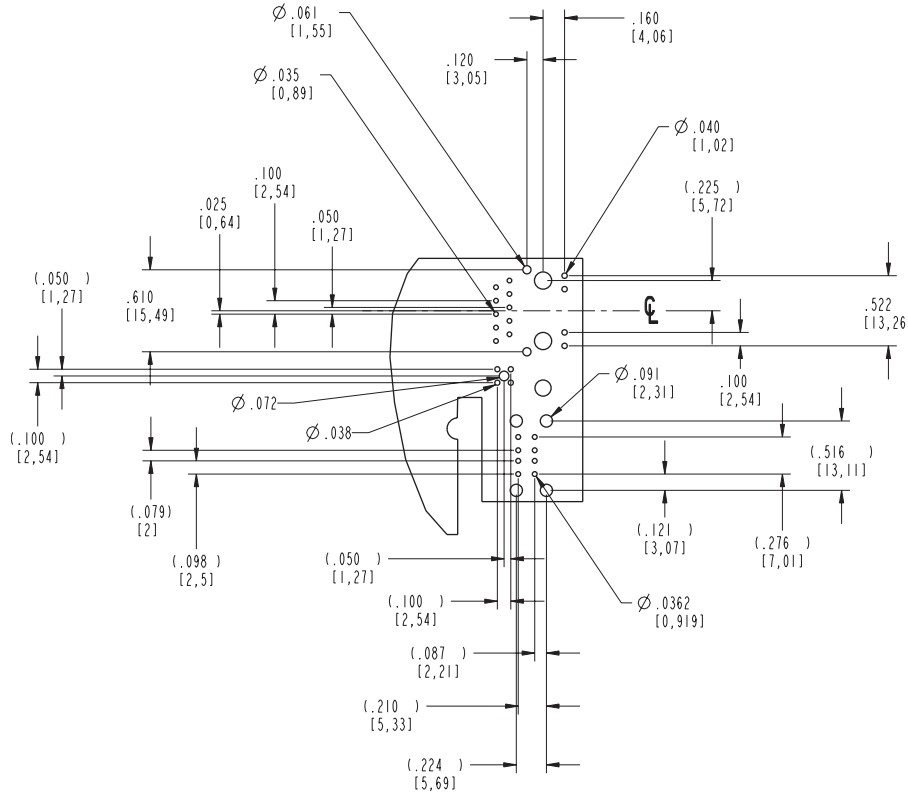
This top view of the module shows the overall dimensions in inches.



Pin locations



Detail of where pins are located



Certifications

APPENDIX B

The ConnectCore 9C products comply with the standards cited in this section.

FCC Part 15 Class B

Radio Frequency Interface (RFI) (FCC 15.105)

The ConnectCore 9C has been tested and found to comply with the limits for Class B digital devices pursuant to Part 15 Subpart B, of the FCC rules. These limits are designed to provide reasonable protection against harmful interference in a residential environment. This equipment generates, uses, and can radiate radio frequency energy, and if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try and correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

Labeling Requirements (FCC 15.19)

This device complies with Part 15 of FCC rules. Operation is subject to the following two conditions: (1) this device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

Modifications (FCC 15.21)

Changes or modifications to this equipment not expressly approved by Digi may void the user's authority to operate this equipment.

Industry Canada

This digital apparatus does not exceed the Class B limits for radio noise emissions from digital apparatus set out in the Radio Interference Regulations of the Canadian Department of Communications.

Le present appareil numerique n'emet pas de bruits radioelectriques depassant les limites applicables aux appareils numeriques de la class B prescrites dans le Reglement sur le brouillage radioelectrique edicte par le ministere des Communications du Canada. (IC (Industry Canada) RSS-210 Issue 5 Section 6.2.2(o))

Declaration of Conformity

(In accordance with FCC Dockets 96-208 and 95-19)

Manufacturer's Name:	Digi International
Corporate Headquarters:	11001 Bren Road East Minnetonka MN 55343
Manufacturing Headquarters:	10000 West 76th Street Eden Prairie MN 55344

Digi International declares, that the product:

Product Name:	ConnectCore 9C
Model Numbers:	50001327-xx

to which this declaration relates, meets the requirements specified by the Federal Communications Commission as detailed in the following specifications:

- Part 15, Subpart B, for Class B equipment
- FCC Docket 96-208 as it applies to Class B
- Personal computers and peripherals

The product listed above has been tested at an External Test Laboratory certified per FCC rules and has been found to meet the FCC, Part 15, Class B, Emission Limits. Documentation is on file and available from the Digi International Homologation Department.

International EMC Standards

The ConnectCore 9C meets the following electromagnetic emissions standards:

- AS/NZS CISPR 22:2002
- ICES-003
- EN 55024

Safety Standards

The ConnectCore 9C meets the following safety standards:

- UL/CUL 60950-1
- IEC/EN 60950-1

Index

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M

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P

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V

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