RIO Application Kit

Hardware Reference

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1 Overview

This document describes the RIO Application Kit hardware board. This board will be referred to hence forth as RIO_APPKIT.

The RIO_APPKIT provides in port expander mode up to 36 input/output signals usable as a maximum of 32 outputs and/or up to 36 input signals depending on the bus mode used to connect the kit to a JumpStart board expansion connector. This can be an SPI serial connector or a parallel connector using 8-bit data bus and control signals wired to universal connector P2.

The RIO_APPKIT is designed to be connected to the peripheral connector of a ConnectCore 9P 9360, ConnectCore Wi 9C, ConnectCore 9P 9215, or ConnectCore 9M2443 JumpStart board. The RIO_APPKIT will be powered from the base board.

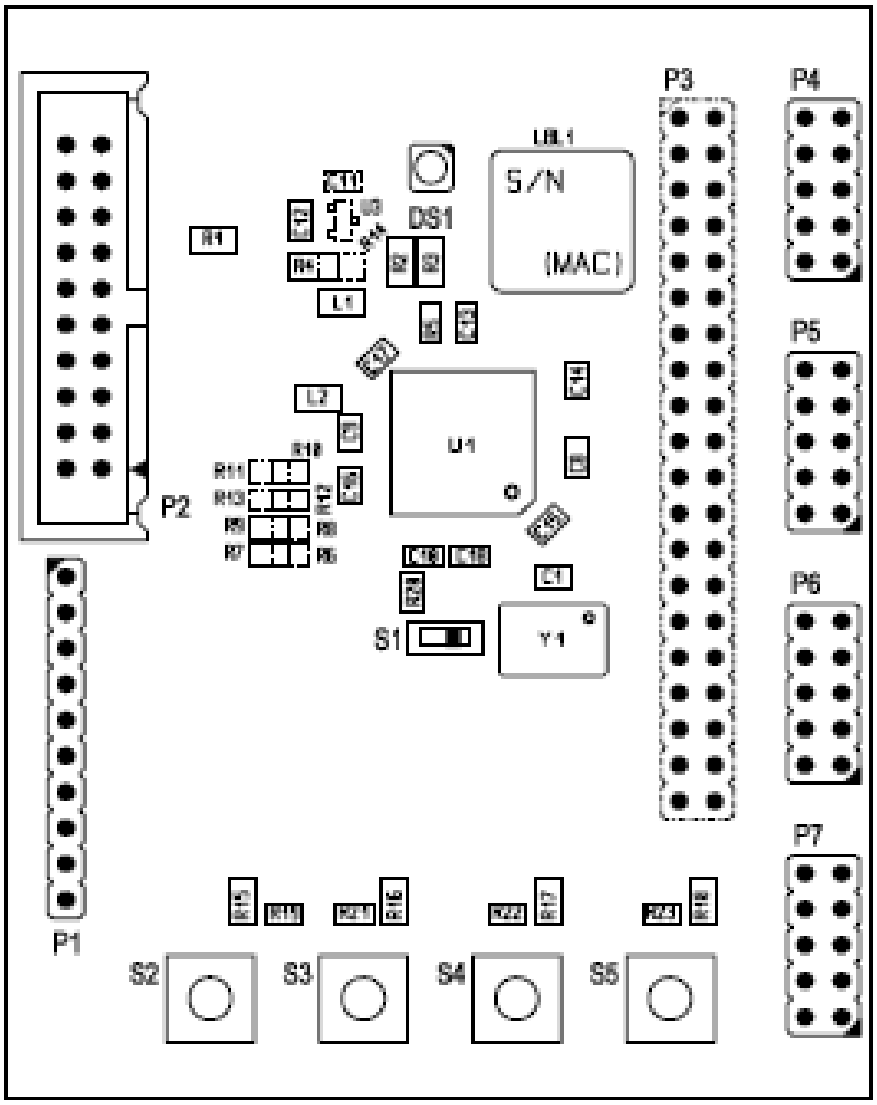
2 Features

The following are major features of the RIO_APPKIT board:

- Eight 4-bit ports usable in six different port modes (digital input, digital output, PWM out, PWM out with phase shift, capture input, quadrature decoder)
- Four additional digital inputs only
- Additional pins for parallel control
- Mode settable by configuration pins
- Up to 40MHz internal or external clock
- Up to 5M baud in serial mode
- Interrupt and GSYNC function
- Configurable 3-wire or 4-wire SPI mode
- Configurable termination resistor for the RS485/422 ports
- Four 10 pin flat cable connectors
- Optional 36 pin port and control signal connector
- Header connector pin to pin compatible with the SPI connectors from ConnectCore 9P 9360, ConnectCore Wi9C and ConnectCore ME JumpStart boards
- ±15kV ESD protection

3 Basic description

The following figure shows the placement of the RIOAPJS_0 board.



4 Connection to development board

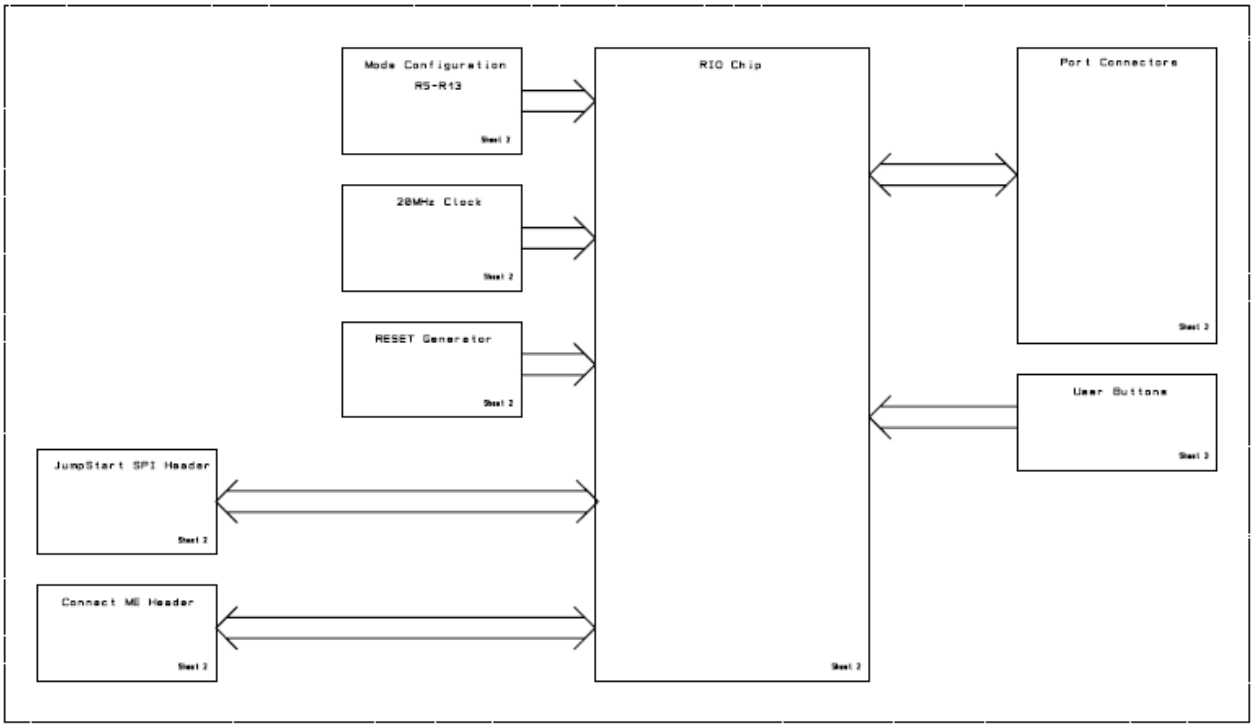
The RIO_APPKIT_0 board has two connectors, P1 and P2 for connecting the kit to the JumpStart boards. Depending on the Jumpstart board used the flat ribbon cable must be connected to a different connector in the RIO_APPKIT.

The following table shows the correspondence between the connectors of the RIO_APPKIT and the supported kits.

JumpStart Kit	Connector
ConnectME	P3
CC9P9360	X8
CC9C / CCWi9C	P7
CC9M2443	X8
CC9P9215	X8

5 Detailed description

5.1 Block diagram



5.2 RIO Chip

The RIO_APPKIT board includes one RIO chip to provide up to 36 additional ports. The RIO is used in port expander mode only. RabbitNet device mode and RabbitNet hub mode are not supported (for details see RIO data sheet).

The RIO chip is connected to the CPU on the base boards either in parallel or serial bus mode (depending on configuration of the RIO_APPKIT). Parallel bus mode can be used wiring signals at P2. Serial bus mode can be used in 3-wire or 4-wire SPI bus mode with both endian modes (LSB or MSB first).

5.2.1 RIO Bus Modes, Parallel Bus Mode

RIO has an asynchronous 8-bit bus with 8 data lines D0..D7 and IOCS#, IORD#, IOWR#, INT#, WAIT# control signals (needs SER/PAR# set to low). Can be used when wiring signals via P2.

5.2.2 Rio Bus Modes, Serial Modes

There are two serial bus modes possible:

1. 4-wire SPI Bus mode with SPI_EN#, SPI_CLK and two unidirectional data lines SPI_DI and SPI_DO
2. 3-wire SPI bus mode with SPI_EN#, SPI_CLK and one bidirectional SPI_DAT line. RABBIT names this mode I2C, but the protocol is different.

SPI_CLK speed can be up to one fourth of the RIO Clock. The endianness (LSB/MSB first) can be set by the configuration input CHA0.

5.3 Ports and RIO Mode

RIO chip has 8 channels with 4 universal port lines each and some additional signal pins with more restricted alternative modes. Further some inputs select the different modes and/or bus modes. Some pins functions depend on the selected RIO mode or bus mode. See table below:

Port	Type	Function Parallel Bus	Function Serial Bus
RC0P0	I/O	RC0P0	RC0P0
RC0P1	I/O	RC0P1	RC0P1
RC0P2	I/O	RC0P2	RC0P2
RC0P3	I/O	RC0P3	RC0P3
RC1P0	I/O	RC1P0	RC1P0
RC1P1	I/O	RC1P1	RC1P1
RC1P2	I/O	RC1P2	RC1P2
RC1P3	I/O	RC1P3	RC1P3
RC2P0	I/O	RC2P0	RC2P0
RC2P1	I/O	RC2P1	RC2P1
RC2P2	I/O	RC2P2	RC2P2
RC2P3	I/O	RC2P3	RC2P3
RC3P0	I/O	RC3P0	RC3P0
RC3P1	I/O	RC3P1	RC3P1
RC3P2	I/O	RC3P2	RC3P2
RC3P3	I/O	RC3P3	RC3P3
RC4P0	I/O	RC4P0	RC4P0
RC4P1	I/O	RC4P1	RC4P1
RC4P2	I/O	RC4P2	RC4P2
RC4P3	I/O	RC4P3	RC4P3
RC5P0	I/O	RC5P0	RC5P0
RC5P1	I/O	RC5P1	RC5P1
RC5P2	I/O	RC5P2	RC5P2
RC5P3	I/O	RC5P3	RC5P3
RC6P0	I/O	RC6P0	RC6P0
D3/RC6P1	I/O	D3	PC6P1
D4/RC6P2	I/O	D4	PC6P2
D4/RC6P3	I/O	D5	PC6P3
RC7P0	I/O	RC7P0	RC7P0
D0/RC7P1	I/O	D0	PC7P1
D1/RC7P2	I/O	D1	PC7P2
D2/RC7P3	I/O	D2	PC7P3

Port	Type	Function Parallel Bus	Function Serial Bus
SERI/D6	I/O	D6	SERI
SERCLK/D7	I/O	D7	SERCLK
GSYNC	I	GSYNC	GSYNC
SER/PAR#	I	Pulled down	Pulled up
WAIT#/SERO	O	WAIT#	SERO
INT#	O	INT#	INT#
IORD#/GPIN4	I	IORD#	GPIN4
IOWR#/GPIN3	I	IOWR#	GPIN3
CS#	I	PARCS#	SERCS#
P#/I	I	Address	Serial mode
G/C#	I	Address	Pulled up
CHA0	I	Address	Serial mode
CHA1/GPIN1	I	Address	GPIN1
CHA2/GPIN2	I	Address	GPIN2
CLK	I	20MHz	20MHz
RESET#	I	RESET#	RESET#

Signal Types:

I/O = Input/Output

I = Input

O = Output

OD = Digital Output, Open Drain

Signal names with more than one function are separated with a “/”

5.4 Port Functions

Every port pin can be configured to different functions:

1. Digital In
2. Digital Out
3. PWM Out
4. PWM Out with Phase Shift
5. Pin Pair Protection
6. Capture Input
7. Quadrature Decoder

The upper two or the lower two bits of one channel can be set to a “safe” output mode, a mode that will disable overlapping on states for these two bits. A settable dead time will be inserted into every change to disable short circuits due to power device hold times. This allows simple and safe solutions for digital power stages.

6 Board Description

The board will have a size of 61 X 77 mm with no prototyping area on this board.

6.1 P1: SPI and additional Signal Connector

2.54mm pitch 10 pole, one row. Fits to SPI connector X8 from JumpStart board with pins 1-6. For stand alone connection in serial SPI bus mode. Other boards can be connected using single wires with 0.635mm sockets.

Pin	Type	Name	Comment
1	P	+3.3V	VDDINT, default VDDIO
2	I	SPIB_DO	
3	O	SPIB_DI	
4	I	SPIB_CLK	
5	I	SPIB_EN#	
6	P	GND	
7	P	+5V	Optional VDDIO
8	I	EXT_RESET#	0R resistor
9	I	EXT_CLK	
10	O	EXT_INT#	0R resistor

6.2 P2: ME SPI and 3.3V Connector

Fits to modem/GPIO connector P3 from ME dev board. For stand alone connection in serial SPI bus mode.

Pin	Type	Name	Comments	Pin	Type	Name	Comments
1	-	n.c.		2	-	n.c.	
3	-	n.c.		4	-	n.c.	
5	-	n.c.		6	-	n.c.	
7	O	SPIB_DI		8	I	SPIB_DO	
9	I	SPIB_CLK		10	-	n.c.	
11	-	n.c.		12	-	n.c.	
13	I	SPIB_EN#		14	I	EXT_REXET#	
15	P	+3.3V		16	P	GND	
17	-	n.c.		18	-	n.c.	
19	-	n.c.		20	O	EXT_INT#	

6.3 P3: RIO GPIO and VDDIO Power Connector

All RIO signals except serial bus signals. Allows usage of parallel bus.

Pin	Type	Name	Comments	Pin	Type	Name	Comments
1	P	GND		2	P	VDDIO	
3	I/O	RC0P0		4	I/O	RC0P1	
5	I/O	RC0P2		6	I/O	RC0P3	
7	I/O	RC1P0		8	I/O	RC1P1	
9	I/O	RC1P2		10	I/O	RC1P3	
11	I/O	RC2P0		12	I/O	RC2P1	
13	I/O	RC2P2		14	I/O	RC2P3	
15	I/O	RC3P0		16	I/O	RC3P1	
17	I/O	RC3P2		18	I/O	RC3P3	
19	I/O	RC4P0		20	I/O	RC4P1	
21	I/O	RC4P2		22	I/O	RC4P3	
23	I/O	RC5P0		24	I/O	RC5P1	
25	I/O	RC5P2		26	I/O	RC5P3	
27	I/O	RC6P0		28	I/O	RC6P1	
29	I/O	RC6P2		30	I/O	RC6P3	
31	I/O	RC7P0		32	I/O	RC7P1	
33	I/O	RC7P2		34	I/O	RC7P3	
35	I	CHA1/GPIN1		36	I	CHA2/GPIN2	
37	I	IOWR#/GPIN3		38	I	IORD#/GPIN4	
39	O	GSYNC		40	-	n.c.	

6.4 P4: P0, P1 Connector

Pin compatible to RABBIT RIO kit.

Pin	Type	Name	Comments	Pin	Type	Name	Comments
1	I/O	RC1P3		2	I/O	RC1P2	
3	I/O	RC1P1		4	I/O	RC1P0	
5	I/O	RC0P3		6	I/O	RC0P2	
7	I/O	RC0P1		8	I/O	RC0P0	
9	P	GND		10	P	VDDIO	

6.5 P5: P2, P3 Connector

Pin compatible to RABBIT RIO kit.

Pin	Type	Name	Comments	Pin	Type	Name	Comments
1	I/O	RC3P3		2	I/O	RC3P2	
3	I/O	RC3P1		4	I/O	RC3P0	
5	I/O	RC2P3		6	I/O	RC2P2	
7	I/O	RC2P1		8	I/O	RC2P0	
9	P	GND		10	P	VDDIO	

6.6 P6: P4, P5 Connector

Pin compatible to RABBIT RIO kit.

Pin	Type	Name	Comments	Pin	Type	Name	Comments
1	I/O	RC5P3		2	I/O	RC5P2	
3	I/O	RC5P1		4	I/O	RC5P0	
5	I/O	RC4P3		6	I/O	RC4P2	
7	I/O	RC4P1		8	I/O	RC4P0	
9	P	GND		10	P	VDDIO	

6.7 P7: P6, P7 Connector

Pin compatible to RABBIT RIO kit.

Pin	Type	Name	Comments	Pin	Type	Name	Comments
1	I/O	RC6P3		2	I/O	RC7P2	
3	I/O	RC6P1		4	I/O	RC6P0	
5	I/O	RC7P3		6	I/O	RC7P2	
7	I/O	RC7P1		8	I/O	RC7P0	
9	P	GND		10	P	VDDIO	

6.8 VDDINT/VDDIO Separation

RIO GPIOs can be used with 3.3V or 5V for VDDIO. VDDINT(core) must always have 3.3V. +3.3V and +5V are accessible at P1. If using 3.3V only supply R4 is populated (default).

Optionally a LDO regulator U3 can be mounted to generate 3.3V core voltage from 5V when using 5V only supply. R4 must be depopulated.

LE1 indicates 3.3V.

6.9 External Clock

Internal RIO clock is generated by a 20MHz oscillator. S1.1 must be closed and S1.2 opened. An external clock from P1 can be used by closing S1.1 and opening S1.2.

6.10 Mode Selection Field

R6-R13 resistors allow selection of RIO mode without using external signals. Pull ups and pull down resistors are weak, so they will be overridden when external signals are connected. Default mode is bold.

Mode	SER/PAR#	G/C#	CHA0	P/I#
Parallel Mode	0	X	X	X
RabbitNet Device	1	0	X	0
RabbitNet Hub	1	0	X	1
SPI2, LSB first	1	1	0	0
SPI1, LSB first	1	1	0	1
SPI2, MSB first	1	1	1	0
SPI1, MSB first	1	1	1	1

SPI1 = bidirectional data line SPI_DAT

SPI2 = unidirectional SPI_SI and SPI_DO

R6,8,10,12 are pull downs, R7,9,11,13 are pull ups

6.11 RESET# Generation

An RC combination generates RESET# at power up. Input EXT_RESET# at P1 pin 8 or P2 pin 14 allows external RESET control.

6.12 Interrupts

The global interrupt output RINT# from RIO can be routed to any suitable input of the application from pin 10 of P1.

6.13 4 User Buttons

4 user buttons S2-S5 are connected to GPIN1-GPIN4. The connection can be opened by removing R15-R18