LM5070 "AE" Evaluation Board

National Semiconductor
Application Note 1358
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Introduction

The LM5070 AE (Area Efficient) evaluation board is designed to provide an IEEE802.3af compliant, Power over Ethernet (PoE) power supply. The power supply features the LM5070 PoE powered device (PD) interface and controller integrated circuit (IC) configured in the versatile flyback topology. The board features a fully isolated solution, but you have the freedom to transform the circuit into a non-isolated regulator if you desire. Several schematic versions are supplied in this document to those ends.

General performance features of the AE evaluation board are:

- Isolated 3.3V output
- Input range: 32 to 57V
- Output current: 0 to 3.3A
- Measured converter efficiency: 84% at 3.0A
- Operating frequency: 250kHz
- Programmed undervoltage lockout (UVLO) release: 38.6V
- Programmed UVLO: 32.4V (6.2V Hysteresis)

A Note About Potentials

The LM5070 is designed to work with PoE applications that are typically -48V systems. The datasheet for the LM5070 was written under the more generic, and more easily understood, positive voltage convention referenced to the V_{EE} pin of the IC. The application board is an example of a PoE system architecture, and has pins “GND” and “$-V_{IN}$” for the high and low input potentials, respectively, and output pins “Vout+” and “SGND”. For simplicity and consistency with the datasheet, this application note will be written and all measurements will be taken using the positive voltage convention, with the “$-V_{IN}$” pin connected to the bench power supply ground, and the GND pin connected to the power supply high potential. Input bridge rectifiers allow either polarity operation when using the RJ-45 connector.

Signature Discovery Mode

To detect a powered device connected to the Ethernet cable, the Power Sourcing Equipment (PSE) will apply two different voltages between 2.8V and 10V across the input terminals of the PD. A PD will be considered present if the detected differential impedance is above 23.75kΩ and below 26.25kΩ If the impedance is less than 15kΩ or greater than 33kΩ, a PD will be considered not present and will not receive power. Impedances between these values may or may not indicate the presence of a valid PD. The LM5070 will enable the signature resistor (R5) at an input voltage of 1.5V, and disable signature mode around 12V, measured at the input pins of the IC. The actual differential threshold voltages measured at the PD board terminals will be somewhat higher (~1.0V) due to the input diodes that are in series with the input.

Classification Mode

To classify the PD according to power draw, the PSE will present a voltage between 14.5V and 20.5V to the PD. The LM5070 enables classification mode at a nominal input voltage of 11.7V, again measured at the input pins of the IC. An internal 1.5V linear regulator (referenced to V_{EE}) and an external resistor connected between the R_{CLASS} pin and VEE provide classification programming current. The following table can be used to select the proper R_{CLASS} resistor.

TABLE 1.

Class	P_{MIN}	P_{MAX}	ICLASS (MIN)	ICLASS (MAX)	RCLASS
0	0.44W	12.95W	0mA	4mA	Open
1	0.44W	3.84W	9mA	12mA	150Ω
2	3.84W	6.49W	17mA	20mA	82.5Ω
3	6.49W	12.95W	26mA	30mA	53.6Ω
4	Reserved	Reserved	36mA	44mA	38.3Ω

As seen on the board schematic, no resistor is needed to program class 0 (full power) because the bias current of the IC (~600µA) will be considered class 0 without any additional current draw.

UVLO and UVLO Hysteresis

The UVLO threshold and UVLO hysteresis can be programmed completely independently of each other. UVLO hysteresis is accomplished with an internal 10uA current source that is switched on and off into the impedance of the UVLO set point resistor divider. When the UVLO pin exceeds 2.00V, the current source is activated to instantly raise the voltage at the UVLO pin. When the UVLO pin voltage falls below the 2.00V threshold, the current source is turned off, causing the voltage at the UVLO pin to fall. The LM5070 UVLO thresholds cannot be programmed lower than 23V, otherwise the device would operate in classification mode with both the classification current source and the SMPS enabled. The combined power dissipation of these two functions could exceed the maximum power dissipation of the package.

Without taking into account the external diodes, UVLO is programmed on the AE board to 31.4V, with 6.2V of hysteresis. UVLO will therefore release at 37.6V. The input steering diodes will add approximately 1V to each threshold, so the UVLO and UVLO release thresholds will be 32.4V and 38.6V, measured at the input connector, respectively.

Inrush Current Limiting

The LM5070’s default inrush current can be as high as 400mA at room temperature. With 20Ω effective series resistance in the input line, an 8V drop may occur at startup. When all tolerances are taken into consideration, it is difficult

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Inrush Current Limiting (Continued)

to guarantee a minimum of 8V of hysteresis while staying within the threshold limits of the IEEE specification. Also, margin between the minimum hysteresis designed and the maximum required is an important design constraint. To lessen the hysteresis requirement, one should program the inrush current to a lesser value.

On the AE application board, the inrush current has been programmed to 150mA using the following equation:

$$RCLP = \frac{16\ k\Omega \times A}{I_{LIMIT}^{inrush}(A)} = \frac{16\ k\Omega \times A}{0.150A} = 107\ k\Omega$$

Taking 20% current programming accuracy into consideration, programming the current limit to 150mA decreases the hysteresis requirement to 3.6V, and a much more robust design is now possible. Programming the inrush current does not affect the power delivering capability during normal operation because the current limit level is switched back to the default level at the end of the inrush sequence.

Flyback Theory of Operation

The flyback transformer is actually a coupled inductor with multiple windings wound on a single gapped core. For simplification, we refer to the first, driven winding, as the primary and the main output winding as the secondary winding of the flyback transformer.

The flyback converter is a converter in which inductive energy is stored by applying a voltage across the primary in a similar manner to that of a boost converter. A second coupled winding (secondary) of the inductor transfers the energy to a secondary side rectifier after the primary voltage has been switched off. This allows the converter input and output grounds to be configured either isolated or non-isolated. A voltage / current ratio transformation is possible by altering the winding ratio between the primary and any other winding. A semi-regulated auxiliary winding can also be provided to bias primary or secondary control circuits.

The transformer's primary inductance is typically designed as large as is practical. However, the air gap necessary to store the cycle energy lowers the obtainable inductance. The higher the primary inductance, the less input ripple current will be generated and the less input filtering will be required.

As shown, the LM5070 directly drives a MOSFET switch to apply voltage across the primary. When the switch turns off, the secondary applies a forward current to the output rectifier and charges the output capacitor. In applications where the input voltage is considerably higher than the output voltage, the turns ratio between primary and secondary will reflect the input/output voltage ratio and the duty cycle.

The LM5070 controller provides an internal startup regulator (V_{CC}), soft start, and over-current protection. The controller can and will run indefinitely without the winding, but the increase in on chip power dissipation will decrease efficiency and may reduce the maximum ambient operating temperature.

Proper Board Connections

Be sure to choose the correct wire size when connecting the source supply and load. Monitor the current into and out of the unit under test (UUT). Monitor the voltages directly at the board terminals, as resistive voltage drops along the wires may decrease measurement accuracy. These precautions are especially important during measurement of conversion efficiency.

Source Power

To fully test the LM5070 evaluation board, a DC power supply capable of at least 60V and 1A is required. Adjusting the short circuit current limit on the power supply to ~1A may prevent board damage if an errant connection is made during evaluation.

Loading / Current Limiting Behavior

A resistive load is optimal, but an appropriate electronic load specified for operation down to 2.0V is acceptable. The maximum load current is 3.4A, exceeding this current at low line may cause oscillatory behavior as the part will go into current limit mode. Current limit mode is triggered any time the average current through the main internal circuit breaker MOSFET exceeds 390mA. If current limit is triggered, the switching regulator is automatically disabled by discharging the softstart pin. The module is then allowed to restart, but the part will reset itself indefinitely if the condition causing the current limit to trip remains.

Power Up

It is suggested that the load be kept reasonably low during the first power up. Check the supply current during signature and classification modes before applying full power. During signature mode, the module should have the I-V characteristics of a 25kΩ resistor in series with two diodes. During classification mode, current draw should be about 600µA at 15V as the R_{CLASS} pin is left open to default to class 0. If the proper response is not observed during both signature and classification modes, check the connections closely.

Once proper setup has been established, full power (48V) may be applied. A voltmeter across the output terminals, V_{out}+ and SGND, will allow direct measurement of the 3.3V output line. Because the output voltage is isolated, it cannot be measured by a meter referenced to the bench power supply ground. If 3.3V is not observed within a few seconds, turn the power supply off and review connections.

A final check of efficiency is the best way to confirm that the UUT is operating properly. Few parameters can be incorrect in a switching power supply without creating additional losses and potentially damaging heat. Efficiency above 70% is expected.

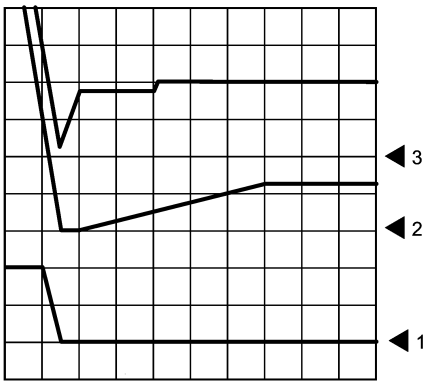
Performance Characteristics

POWER UP SEQUENCE

In addition to a reduction in board area, the high level of integration designed into the LM5070 allows all power sequencing communications to occur within the IC. Very little system management design is required by the design engineer. The power up sequence is as follows:

1. Before power up, all nodes in the non-isolated section of the power supply remain at high potential until UVLO is released and the drain of the main circuit breaker internal MOSFET is pulled down to V_{EE} (IC pin 7).
2. Once the RTN pin of the IC (pin 8) drops below 1.5V (referenced to V_{EE}), the V_{CC} regulator is released and allowed to start. This signals the assertion of the internal "Power Good" signal. The V_{CC} regulator ramps at a rate equal to its current limit, typically 20 mA, divided by the V_{CC} load capacitance.
3. Once the V_{CC} regulator is within minimum regulation, about 7.9V referenced to RTN, the softstart pin is released. The softstart pin will rise at a rate equal to the softstart current source, typically 10µA, divided by the softstart pin capacitance.
4. As the switching regulator achieves regulation, the auxiliary winding will raise the V_{CC} voltage to ~12V, thus shutting down the internal regulator and increasing efficiency.

Figure 1 shows the RTN, V_{CC}, and Softstart IC pins during a normal startup sequence. The auxiliary winding starts to supply a higher voltage to V_{CC} as the switching regulator output voltage rises.



Horizontal resolution: 5 ms/Div.
Trace 1: RTN pin, elevated until UVLO release 20.0 V/Div.
Trace 2. Softstart pin, starts when V_{CC} achieves minimum regulation, 5.0 V/Div.
Trace 3: V_{CC}, starts when RTN < 1.5V, elevated by auxiliary winding, 5.0 V/Div.

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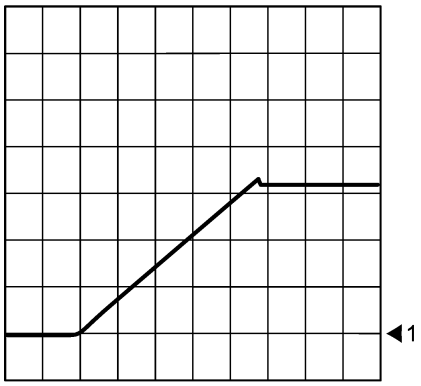
FIGURE 1. Normal Startup Sequence

Figure 2 shows a normal 3.3V line startup.



Horizontal Resolution: 1.0 ms/Div.
Trace 1: +3.3V output line, 1.0V/Div

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FIGURE 2. Regulator Output (+3.3V) Startup Detail

OUTPUT DEAD SHORT FAULT RESPONSE

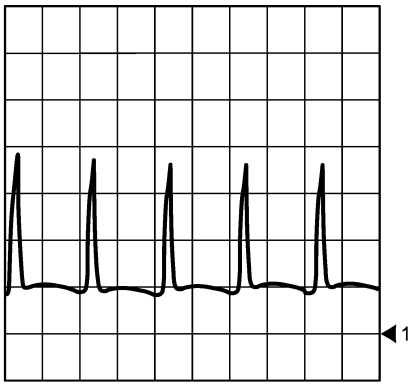
The system should be able to survive a dead short at the output. Applying a dead short to the +3.3V line causes a number of protection mechanisms to trip sequentially. They are:

1. Feedback raises duty cycle in an attempt to maintain the output voltage. This causes a cycle-by-cycle overcurrent condition to exist at the programmable current sense (CS) pin of the IC.
2. The average current in the internal circuit breaker MOSFET rises until it is current limited around 390mA. Some overshoot in the current will be observed, as it takes time for the current limit amplifier to react and change the operating mode of the MOSFET.
3. Because linear current limit is accomplished by driving the MOSET into saturation, the drain voltage (RTN pin) rises. When it reaches 2.5V with respect to V_{EE}, the internal Power Good signal is de-asserted.
4. The de-assertion of Power Good causes the discharge of the Softstart pin, which disables all switching action.
5. Once the switching action stops, the fault condition is no longer observed by the LM5070, and the system is allowed to automatically restart when Power Good is re-asserted.

Performance Characteristics

(Continued)

The AE board has a programmed switching regulator current limit of 1.5A, not high enough to cause an over current condition in the circuit breaker MOSFET. Consequently, steps 2-5 above will not be observed and the module will remain in cycle-by-cycle current limit indefinitely until the fault condition is removed. Changing the current sense resistor to a lower value may induce automatic re-try mode per steps 1-5. Figure 3 shows the CS pin during an output short condition.



Horizontal Resolution: 2.0 μs/Div.
Trace 1: CS pin, 200 mV/Div.

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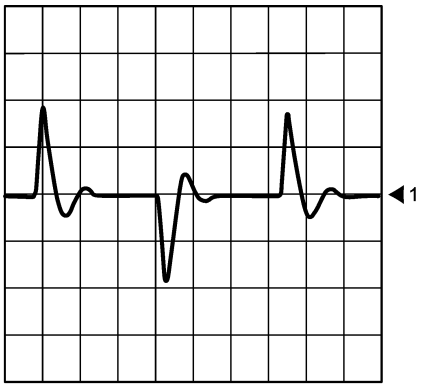
FIGURE 3. CS Pin During Output Short Fault

STEP RESPONSE

Figure 4 shows the step response at V_{IN} = 48V for an alternating instantaneous load change from 1A to 3A.



Horizontal Resolution: 200.0 μs/Div.
Trace 1: +3.3V Output (AC coupled), 100 mV/Div.

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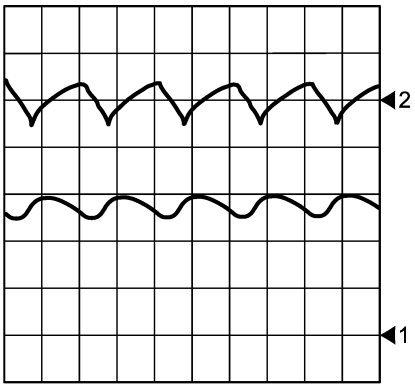
FIGURE 4. Regulator Response to Step Load

Performance Characteristics

(Continued)

RIPPLE VOLTAGE/CURRENTS



Horizontal Resolution: 2.0 μs/Div.
Trace 1 = Input Current Ripple, 100 mA/Div.
Trace 2 = Input Ripple (AC Coupled), 200 mV/Div.

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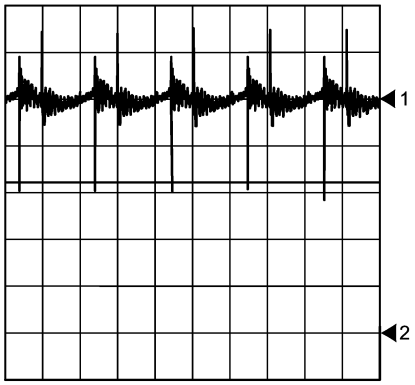
FIGURE 5. Input Ripple



Horizontal Resolution: 2.0 μs/Div.
Trace 1 = Output Ripple (AC Coupled), 20 mV/Div.
Trace 2 = Output Current Ripple, 1.0A/Div.

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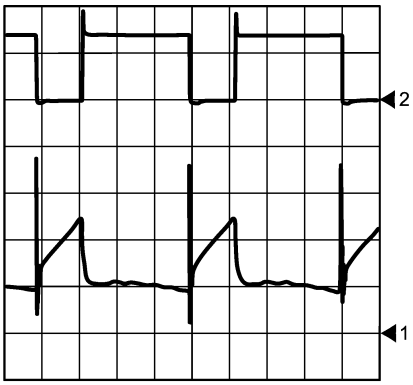
FIGURE 6. Output Ripple

SWITCHING WAVEFORMS



Horizontal Resolution: 1.0 μs/Div.
Trace 1 = CS Pin, 200 mV/Div.
Trace 2 = Drain of MOSFET Q1, 50V/Div.

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FIGURE 7. Typical Switching Waveforms

A Note on the Schematics

The AE evaluation board is typically configured with the output fully isolated from the GND and "-V_{IN}" terminals, though it may be desirable to configure a non-isolated solution in some applications. The board is fully configurable using various jumpers that are preset when the board leaves the factory. Three schematics are supplied to aid the engineer with the design of various configurations. The first is representative of the isolated design, the second a typical non-isolated solution. The last shows the entire configurable board with all jumpers required to design either isolated or non-isolated regulators.

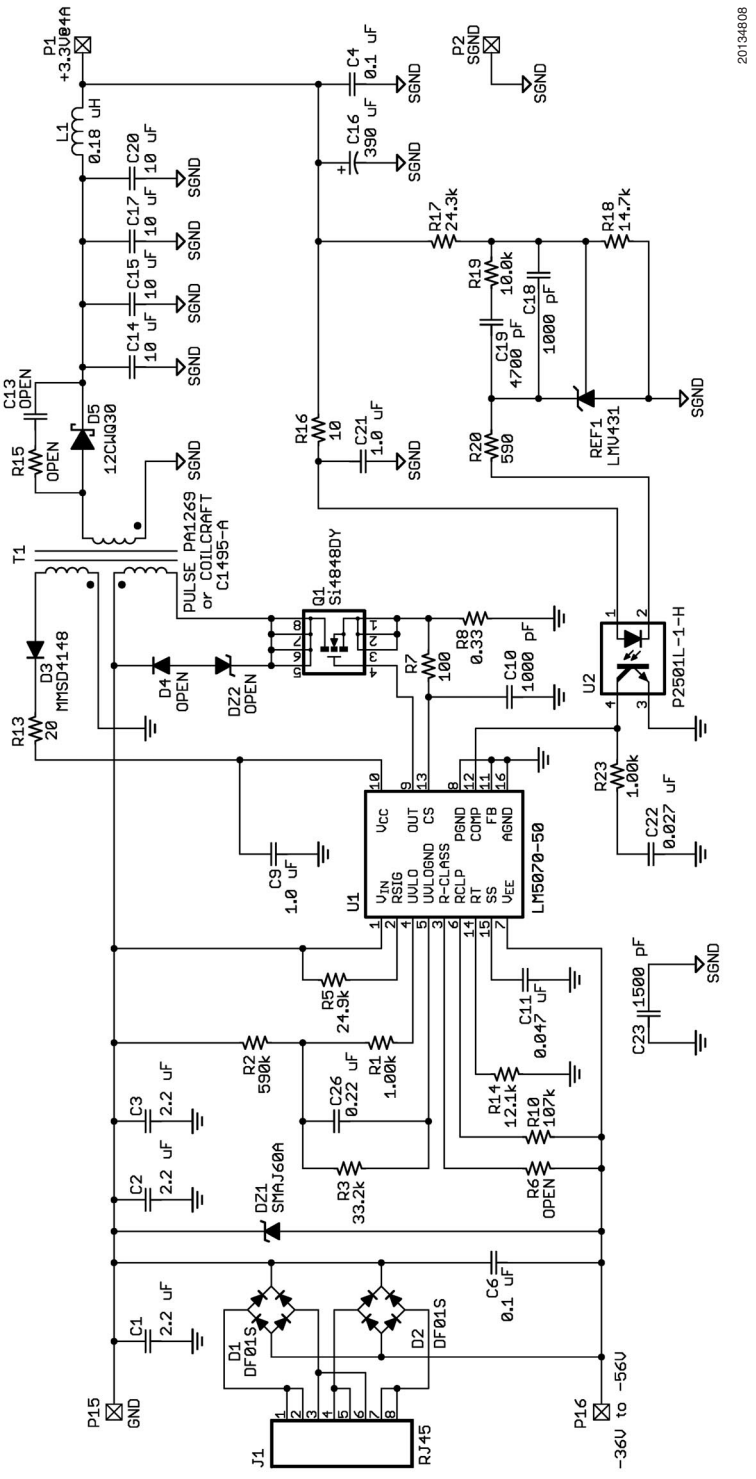

FIGURE 8. Isolated Solution

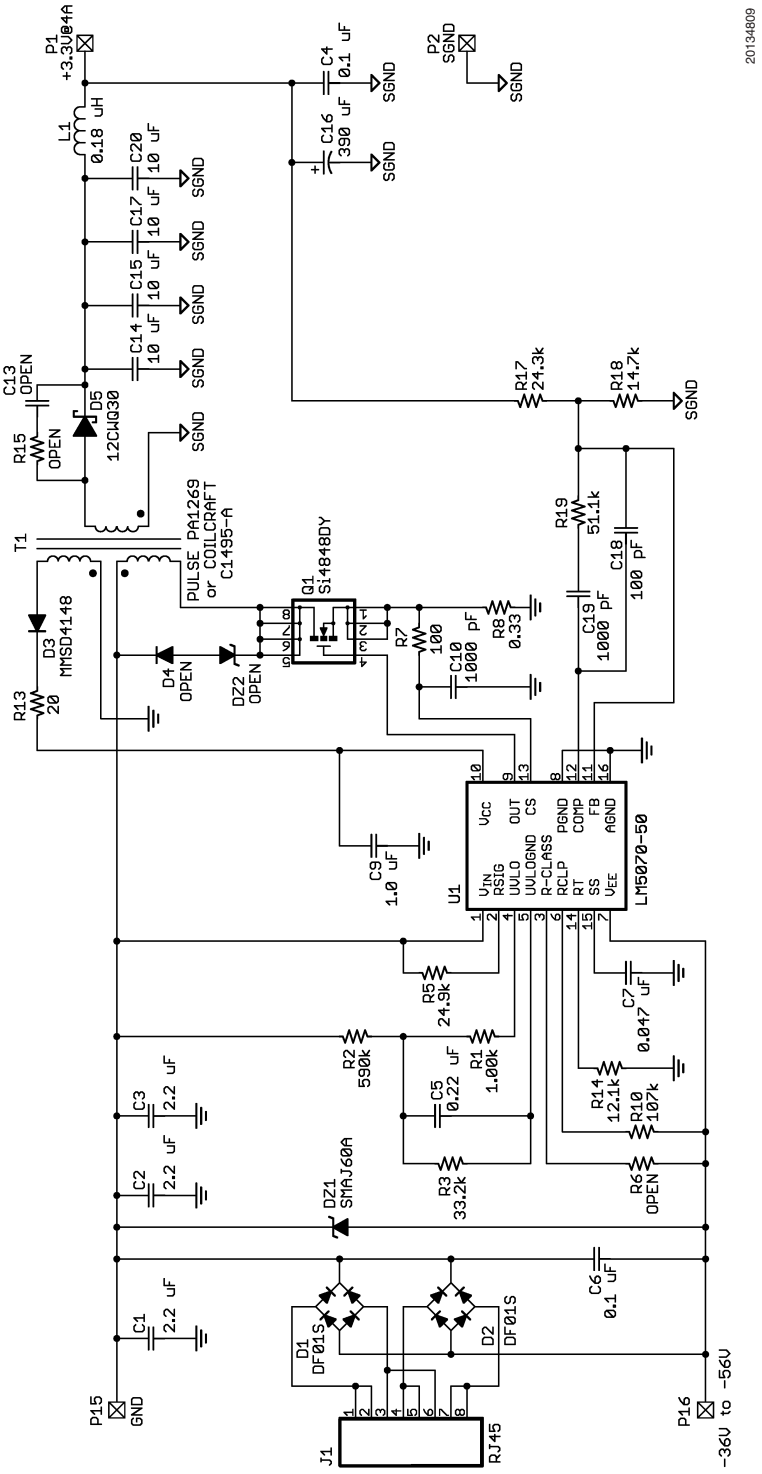

FIGURE 9. Non-Isolated Solution

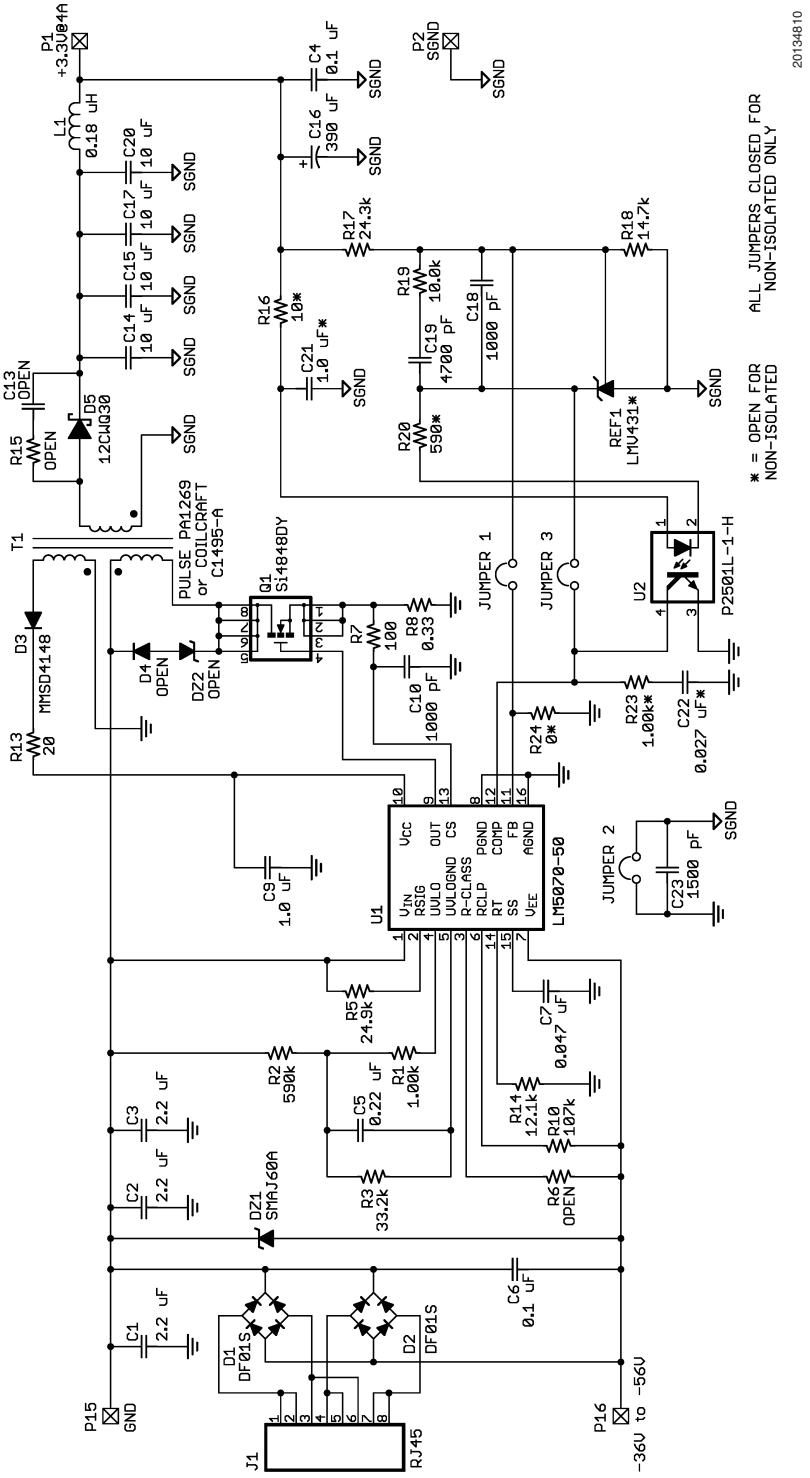

FIGURE 10. Full Board with Jumpers and All Components

Bill of Materials for LM5070 3.3V PoE Isolated Evaluation Board

Designator	Part Type	Footprint	Description	Manufacturer
C1	2.2µ, 100V	1812	Capacitor Ceramic X7R	TDK/C4532X7R2A225
C2	2.2µ, 100V	1812	Capacitor Ceramic X7R	TDK/C4532X7R2A225
C3	2.2µ, 100V	1812	Capacitor Ceramic X7R	TDK/C4532X7R2A225
C4	0.1µ	805	Capacitor Ceramic X7R	Vitramon/VJ0805
C5	0.22µ	805	Capacitor Ceramic X7R	Vitramon/VJ0805
C6	0.1µ	805	Capacitor Ceramic X7R	Vitramon/VJ0805
C7	47n	805	Capacitor Ceramic X7R	Vitramon/VJ0805
C9	1µ	805	Capacitor Ceramic X7R	TDK/C2012X5R1A105K
C10	1n	805	Capacitor Ceramic X7R	Vitramon/VJ0805
C13	OPEN	805		
C14	10µ, 6.3V	1206	Capacitor Ceramic X7R	TDK/C3216X5R0J106K
C15	10µ, 6.3V	1206	Capacitor Ceramic X7R	TDK/C3216X5R0J106K
C16	390u		Capacitor electrolytic	Sanyo/6CV390EX
C17	10µ, 6.3V	1206	Capacitor Ceramic X7R	TDK/C3216X5R0J106K
C18	1n	805	Capacitor Ceramic X7R	Vitramon/VJ0805
C19	4.7n	805	Capacitor Ceramic X7R	Vitramon/VJ0805
C20	10µ, 6.3V	1206	Capacitor Ceramic X7R	TDK/C3216X5R0J106K
C21	1µ	805	Capacitor Ceramic X7R	TDK/C2012X5R1A105K
C22	27n	805	Capacitor Ceramic X7R	Vitramon/VJ0805
C23	1.5n		Capacitor ceramic	Panasonic/ECKANA152ME
D1	DF01S	DFS	Diode bridge	Vishay/DF01S
D1A	HD01	MiniDip	Diode bridge	Diodes Inc/HD01
D2	DF01S	DFS	Diode bridge	Vishay/DF01S
D2A	HD01	MiniDip	Diode bridge	Diodes Inc/HD01
D3	MMSD4148	SOT-23	Small signal diode	Vishay/MMSD4148
D4	OPEN	SOD-123		
D5	12CWQ03	DPAK	Shottky rectifier	IR/12CWQ03
DZ1	SMAJ60A	SMA	Transient suppressor diode	Diodes/SMAJ60A
DZ2	OPEN	SMA	Transient suppressor diode	
J1A	RJ45		Unshielded Ethernet jack	Samtec/MODS-A-8P8C-X
J1B	RJ45		Shielded Ethernet jack	Samtec/MODS-A-8P8C-X-C
JP_1	OPEN			
JP_2	OPEN			
JP_3	OPEN			
L1	0.18µH	DO1813P-181HC	Output inductor	Coilcraft/DO1813P-181HC
Q1	SI4848DY	SO-8	N-channel power MOSFET	Vishay/SI4848DY
R1	1.00k	805	1% Thick Film	DALE CRCW0805
R2	590k	805	1% Thick Film	DALE CRCW0805
R3	33.2k	805	1% Thick Film	DALE CRCW0805
R5	24.9k	805	1% Thick Film	DALE CRCW0805
R6	OPEN	805	1% Thick Film	DALE CRCW0805
R7	100	805	1% Thick Film	DALE CRCW0805
R8	0.33	1210	1% Thick Film	DALE CRCW1210
R10	107k	805	1% Thick Film	DALE CRCW0805
R13	20	805	1% Thick Film	DALE CRCW0805
R14	12.1k	805	1% Thick Film	DALE CRCW0805
R15	OPEN	1210		
R16	10/OPEN for NI	805	1% Thick Film	DALE CRCW0805
R17	24.3k	805	1% Thick Film	DALE CRCW0805

Bill of Materials for LM5070 3.3V PoE Isolated Evaluation Board (Continued)

Designator	Part Type	Footprint	Description	Manufacturer
R18	14.7k	805	1% Thick Film	DALE CRCW0805
R19	10.0k	805	1% Thick Film	DALE CRCW0805
R20	590/OPEN for NI	805	1% Thick Film	DALE CRCW0805
R23	1.00k/OPEN for NI	805	1% Thick Film	DALE CRCW0805
R24	0	805	1% Thick Film	DALE CRCW0805
REF1	LMV431/OPEN for NI	SOT23-5	Precision adjustable shunt regulator	National/LMV431
T1A	Pulse PA1269	EP13	POE Power transformer	Pulse/PA1269
T1B	Coilcraft C1495-A	EP13		Coilcraft/C1495-A
U1	LM5070-50	TSSOP-16	POE PD Interface and PWM Controller	National/LM5070-50
U2	PS2501L-1-H	dip4-smt	Surface mount opto-coupler	NEC/PS2501L-1-H

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