LCD Displays Supported by the NetSilicon NS9750/NS9360 Processors

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Overview

The quality of LCD displays exceeds that of CRT (cathode ray tube) displays. LCD displays are smaller, thinner, and lighter, and they use less power. These displays are ubiquitous in laptops, projectors, PDAs, cell phones, industrial panels, advertisement displays, access control, point of sale, and many other applications. And the majority of devices with displays have already been, or will be, interconnected and connected to other devices within Internet and local area networks.

The NS9750 includes both network connectivity and an LCD controller, and it offers an inexpensive and easy-to-design solution for many applications. The NS9750 LCD controller supports most commercially available graphical (as opposed to alphanumeric) LCD displays.

This document describes display parameters, investigates system limitations, and provides a tool for estimating maximum display size in your own design.

Note that the NS9750 and the NS9360 have very similar timing; the NS9750 is used as an example in this document.

Supported display types

The NS9750 LCD controller is programmable and supports any of the eight basic display categories:

- Two types of color TFT (thin film transistor), also called active matrix (AM):
  - 18-data-pin
  - 24-data-pin direct
- Six types of STN (super twisted nematic), also called passive matrix (PM):
  - Three single-panel
  - Three dual-panel displays

- Each STN display is either color or monochrome:
  - Color display: up to 8-data-pin using color-enhancing palette RAM
  - Monochrome display: up to 8-data-pin or 4-data-pin using gray-scale-enhancing palette RAM

Most 24-bit TFT displays require LVDS (low voltage differential signaling) inputs. These displays typically require an off-the-shelf serializer device such as the National DS90C385 to interface the display to the display controller. The NS9750 LCD controller connects directly to the parallel interface of the serializer. (For recommended devices, contact the LCD display manufacturer.) Other displays either connect directly to NS9750 outputs or require buffers, especially for longer cables between the NS9750 and the display. NetSilicon recommends you use the buffers.

The STN double panel is a single display that is internally divided into two parts, both of which are driven in parallel. STN double panels typically are used with larger size displays that exhibit large capacitive loads; the pixel drivers are too slow to address all pixels in a single frame cycle. This display type is being replaced by TFT displays, which are dropping in price. Two displays could be driven using the double panel mode. We did not test the NS9750 LCD controller with double panel displays.

Passive matrix displays use more power than TFT displays, and they provide a narrower viewing angle and lower contrast ratio. These displays also are being replaced by TFT displays. Low-cost ragged passive matrix displays, however, are still being used in many industrial applications.

Number of data pins

The NS9750 LCD controller has six control pins, described next:

Signal name	Type	Description
CLPOWER	Output	LCD panel power enable
CLLP	Output	Line synchronization pulse (STN)/horizontal synchronization pulse (TFT)
CLCP	Output	LCD panel clock
CLFP	Output	Frame pulse (STN)/vertical synchronization pulse (TFT)
CLAC	Output	STN AC bias drive or TFT data enable output
CLLE	Output	Line end signal

Displays typically require four to six control pins. The number of data pins depends on the display type, as this table shows:

Display type		Number of data pins: panel 1	Number of data pins: panel 2
TFT – color only	Color 24-bit	24	Not applicable
	Color 18-bit	18	Not applicable
STN – color	Single panel 8-bit	8	Not applicable
	Dual panel 8-bit	8	8

STN – monochrome	Single panel 4-bit	4	Not applicable
	Dual panel 4-bit	4	4
	Single panel 8-bit	8	Not applicable
	Dual panel 8-bit	8	8

The double-panel displays use twice as many pins but don't offer more color (or gray) shades.

Number of colors or gray shades

The number of colors or gray shades correlates to the number of data pins, on color processing techniques, data shifting techniques. (For the exact values, see the *NS9750 Hardware Reference*.) The NS9750 controller uses an internal programmable palette-LUT (look-up table) and a grayscaler to support color processing techniques. Sample displays are provided next; the last three listed will be tested with the NS9750 development board.

- The 24-pin TFT display accepts 24 bits at a time. The NS9750 LCD controller transfers all 24 bits from SDRAM and does not use gray-scale-increasing techniques. The resulting number of colors is close to 2*n*, where *n* is the number of bits. For example, a 24-bit display exhibits close to 2 24 colors or 16 million colors. The 24 bits are composed of 8 bits each of RGB (red), G (green) and B (blue) primary colors.
- The 18-pin TFT display, such as the SHARP LQ10D421, accepts 18-color RGB bits (6 bits per color) at a time. The NS9750 LCD controller transfers only 16 bits from SDRAM: 5 bits each for RGB and a single LSB (least significant bit) that is split into three equal values among R, G, and B. This exhibits close to 2 16 = 64 thousand colors.
- The 8-pin STN color display, (for example, the SHARP LM057QC1T01), shifts 8-color bits at a time: RGBRGBRG bits followed by BRGBRGBR bits followed by GBRGBRGB, and so on. The LCD controller provides color enhancing resulting in 3375 color grades.
- The 4-bit STN monochrome display, such as the Grand Pacific Optoelectronics GM0008-13, shifts 4 monochrome bits at a time, resulting in 15 gray shades (24 – 1).

Resolution

The resolution of the NS9750 LCD controller is programmable. NetSilicon supports standard displays with these resolutions:

- QVGA = 320 x 240
- VGA = 640 x 480
- SGA = 800 x 600
- XGA = 1024 x 768

Lower resolution displays also are supported. Displays typically have programmable vertical resolutions within a certain range, especially if they are used for TV displays (to accommodate different TV standards).

Refresh frequency

Refresh frequency is programmable in the NS9750 LCD controller. Lower refresh frequency uses less power but may exhibit flicker; for that reason, laptop screens refresh at higher

rates. TV sets may require a refresh of 50Hz (SECAM, PAL – used in Europe) or 60Hz (NTSC – used in the United States). TFT displays usually exhibit less flicker than STN displays because they have a transistor switch behind each pixel on the screen and can hold capacitive charge longer.

Physical size

The physical size of the display is irrelevant for the LCD controller.

The largest supported displays

To reduce the system cost, the LCD controller uses NS9750 system memory as a video buffer. This design introduced necessary trade-offs between system cost and the resolution of displays that can be supported. The arithmetic product of three parameters limits the display resolution:

```
number of data bits x display resolution x refresh frequency
```

This product must not exceed the NS9750 system bus bandwidth allocated to the display.

Simplified formula

The NS9750 comes in three speed grades; the fastest is 200MHz CPU/ 100MHz system bus speed. This speed grade results in 400MB/s bus bandwidth because the bus is 4 bytes wide. For bandwidth planning, the maximum bandwidth must be reduced to account for overhead and read/write switching. The effective bandwidth is ½ of the system bus bandwidth; that is, 200MB/s. This value is predicted to be the worst case for the NS9750. The NS9750 architecture allocates half of the system bus bandwidth to the CPU. The remaining five bus master peripherals (Ethernet Tx, Ethernet Rx, PCI or CardBus, Peripheral Bus Bridge, and LCD controller) share the other half of the bandwidth. The bandwidth assignment between these peripherals is programmable (patent pending). Using this simple formula, you can estimate the amount of bandwidth available to your LCD display:

CPU bandwidth = `100MB/s`

All other peripherals (including LCD) = `100MB/s`

Be aware that the actual bandwidth used by the display is:

display clock rate X number of hits per clock

For example, a clock rate of 50MHz with 16 bits of color yields a bandwidth of 100 Mbsec. To minimize bandwidth needs, you may need to use an eternal oscillator to get the exact rate.

Sample applications

Case 1: 18-bit VGA

The 18-bit TFT display transfers 16 bits per pixel and generates the last 2 bits inside the LCD controller. This display packs two color RGB pixels into a single 4-byte word.

The 18-bit VGA display (640x480), refreshing 60 times per second, requires 37 MB/s:

```
2 x 640 x 480 x 60 = 37 MB/s
```

67 MB/s are left to all other peripherals. If the LCD refresh frequency increases to 70Hz, its required bandwidth increases to 43 MB/s.

The NS9750 LCD controller supports 18-bit VGA displays in most applications.

Case 2: 24-bit VGA

The 24-bit TFT display requires 4 bytes to transfer one color RGB pixel over the NS9750 bus. The LCD controller does not pack the bytes into 32-bit words; instead, it packs 3 bytes into a 4- byte word and ignores 1 byte.

The 24-bit VGA display (640x480), refreshing 60 times per second, requires 74 MB/s:

```
4 x 640 x 480 x 60 = 74 MB/s
```

26 MB/s are left to other peripherals. If the LCD refresh frequency increases to 70Hz, its required bandwidth increases to 86MB/s.

The NS9750 LCD controller supports 24-bit VGA displays in many applications.

Case 3: 18-bit SGA

The 18-bit SGA display with 60Hz refresh requires 58 MB/s:

```
2 x 800 x 600 x 60 = 58MB/s
```

42 MB/s are left to other peripherals. If your application transfers a new image of this size (that is, 2 x 1024 x 768 = 1.6MB) over 100bT Ethernet in one direction less often than once per second, this display can be supported in your application (see the table in the next section). Lowering the refresh frequency to 50Hz drops the LCD bandwidth requirement to 48 MB/s.

The NS9750 LCD controller can support 18-bit SGA displays in many applications.

Case 4: 18-bit XGA

The 18-bit XGA display with 60Hz refresh requires 94 MB/s:

```
2 x 1024 x 768 x 60 = 94MB/s
```

6 MB/s are left to other peripherals. If your application transfers a new image of this size (that is, 2 x 1024 x 768 = 1.6MB) over 100bT Ethernet in one direction less than once per second, this display can be supported in your application. Lowering the refresh frequency to 50Hz drops the LCD bandwidth requirement to 78 MB/s.

The NS9750 LCD controller can support 18-bit XGA displays only with careful design in special applications that require slow (more than 1s) changes in image.

The physical size of the display is not relevant to these calculations.

The next table summarizes selected cases of bandwidth requirements for high-resolution TFT displays. The lower resolution displays require significantly less bandwidth, so they are supported. STN displays tend to be lower resolution; they are supported as well.

The next table shows high-resolution TFT displays supported by NS9750 with effective system bus bandwidth 200MB/s divided in half between the CPU (100MB/s) and the rest of the peripherals (100MB/s):

Display type	Refresh frequency in HZ	BW required for display in MB/s	BW left to other peripherals in MB/
18b VGA	50	31	69
(640 x 480)	60	37	63
	70	43	57
24b VGA	50	62	38
(640 x 480)	60	74	26
	70	86	14
18b SGA*	50	48	52
(800 x 600)	60	58	42
	70	68	32
24b SGA*		96	4
(800 x 600)			
96 4*	50	78	22
18b XGA	60	94	6
(1024 x 768)	70		

The display types marked with asterisks (*) require the system timing changes described next.

System timing changes

The default LCD controller configuration supported by the NS9360 and NS9750 is 800 X 480 with 8 bits for color. The bandwidth is guaranteed, so the designer does not have to be concerned about bandwidth use. Higher resolutions are possible but require care in their setup and design.

Note that the bandwidth needed is determined by the rate at which the display device requires bits. Each display device can have different bit rate requirements for the same resolution and refresh rate. We have seen up to 2:1 differences between devices with the same resolution. The highest bit rate that doesn't require slowing down CPU accesses is 50 Mb per second, which is sufficient to support some 800 X 640 panels, but not all 800 X 480 displays. To determine the bit rate needed for a particular resolution, refresh rate, and display, you must have a thorough understanding of the display needs as defined in the specification.

The total available bus bandwidth is 160-200 Mb per second shared by the CPU, LCD controller, and all other peripherals, including Ethernet. The highest achievable bit rate is 100 Mb per second for the NS9750, but it requires reducing the amount of bandwidth allowed for the CPU. Some applications may run slowly as the LCD controller can receive most of the bandwidth.

To achieve higher bit rates, set bit 0 in the AHB Arbiter General Configuration register address to 1 to reduce the bandwidth allocated to the CPU. Then, using the mechanism provided in Chapter 4, "System Control Module - Bus Arbiter" of your hardware reference, you can allocate bandwidth to the LCD controller, CPU, and other peripherals. You must ensure that the bandwidth is allocated to meet the needs of the display while allowing enough bandwidth to satisfy the rest of the application.