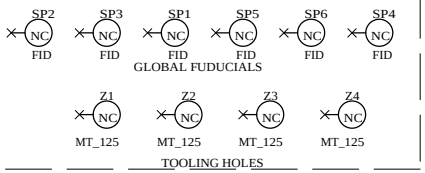
NOTES:

1. ALL RESISTOR VALUES ARE IN OHMS AND IN THE 0603 SIZE UNLESS OTHERWISE NOTED
2. ALL RESISTOR VALUES ARE 5% UNLESS OTHERWISE NOTED
3. ALL CAPACITORS ARE RATED IN uFARADS AND IN THE 0603 SIZE UNLESS OTHERWISE NOTED
4. ALL CAPACITORS ARE RATED AT 50 VDC OR HIGHER UNLESS OTHERWISE NOTED
5. LAST USED:



N20M50Bga

DEVELOPMENT BOARD

BOARD REVISIONS

04/18/02 1951000 REV A
07/23/02 1951001 REV B

BOARD REV NOTES

REB B PCB incorperates REV B SH.13 correction

SHEET REV NOTES

Sh.02 Rev B: Updates PORT Descriptions
Sh.04 Rev B: Updates Table 1 C1 to C22
Sh.08 Rev B: Updates Note for RTSB* 1K pull-down.
Sh.09 Rev B: Updates Note for TXD3:0 Resistors - Sh.01 to Rev C
Sh.12 Rev B: Changes 2.5 regulator Capacitor C10 from 4.7 to 10uF LESR
Sh.13 Rev B: Swapped mis-connected 3.3V & GND pins on U16

SHEET DESCRIPTION

SH. #	REV.	DESCRIPTION
1.	C	Cover Sheet
2.	B	Port & Chip Select Information
3.	A	NETARM BGA & BCLK Buffer
4.	B	Emulator Hdrs., Jtag, & Addr. Buffers
5.	A	Flash, Parallel & Serial EE Memory
6.	A	SDRAM Memory
7.	A	1Mbps Serial Port A(1)
8.	B	1Mbps Serial Port B(2) or RS485
9.	B	Ethernet Front End; 10/100BaseTX
10.	A	ENI/GPIO Port
11.	A	System Bus Expansion Conn. & Dipswitches
12.	B	Power Supply, Breadboard Area, & LEDs
13.	B	NETARM PQFP

REF SCH1951001

DESIGNER: Don Stone

NetSilicon - A Digi International Company, Waltham, MA

Title: NET+ARM 20M/50 COVER SHEET

Size	Document Number	Rev
	n20m50b01.SCH	C

Date: Thursday, September 05, 2002 Sheet 1 of 13

Port A - High Speed RS232 Serial Port with Modem Support

0 DCD* Serial port 1
1 CTS* Serial port 1
2 DSR* Serial port 1
3 RxD Serial port 1
4 Burst Terminate (0 Outside arms burst terminate fix)
5 RTS* Serial port 1
6 DTR* Serial port 1
7 TxD Serial port 1
All 8 bits go to Expansion Connector and can be disabled for off-board use.

Port B - High Speed RS232 Serial Port or RS485

0 General Purpose LED, (0 Outside = LED on)
1 CTS* Serial port 2
2 General Purpose LED, (0 Outside = LED on)
3 RxD Serial port 2/RS485 Input
4 Reset PHY, (0 Outside = reset. Board is Strapped for Hardware RESET)
5 RTS* Serial port 2/ RS485 Driver Enable, (1 Outside = Enable)
6 DTR* Serial port 2/ RS485 Receiver Enable, (0 Outside = Enable)
7 TxD Serial port 2/ RS485 Output
All 8 bits go to Expansion Connector and can be disabled for off-board use.

Port C - Serial EE Memory

0 Interrupt from PHY (input)
1 CPU LED Green, (0 Outside = LED on)
2 CPU LED Yellow, (0 Outside = LED on)
3 Serial EE Clock (output) or AMUX
4 Serial EE (data input)
5 Serial EE (data output)
6 RIA* Serial port 1(Or Serial EE Clock output)
7 Serial EE chip select, (0 Outside = selected)
All 8 bits go to Expansion Connector and can be disabled for off-board use.

For NET+20M to NET+20UM migration only eight(8) of the sixteen(16) combined PORTB and PORTC pins should be used.

Chip Selects

CS0 Flash Memory, x16 or x32, 1-16Mbytes
CS1 SDRAM Memory, x16 or x32, 8-16Mbytes
CS2 Spare to Expansion Connector
CS3 Parallel EE Memory & to Expansion Connector
CS4 Spare to Expansion Connector

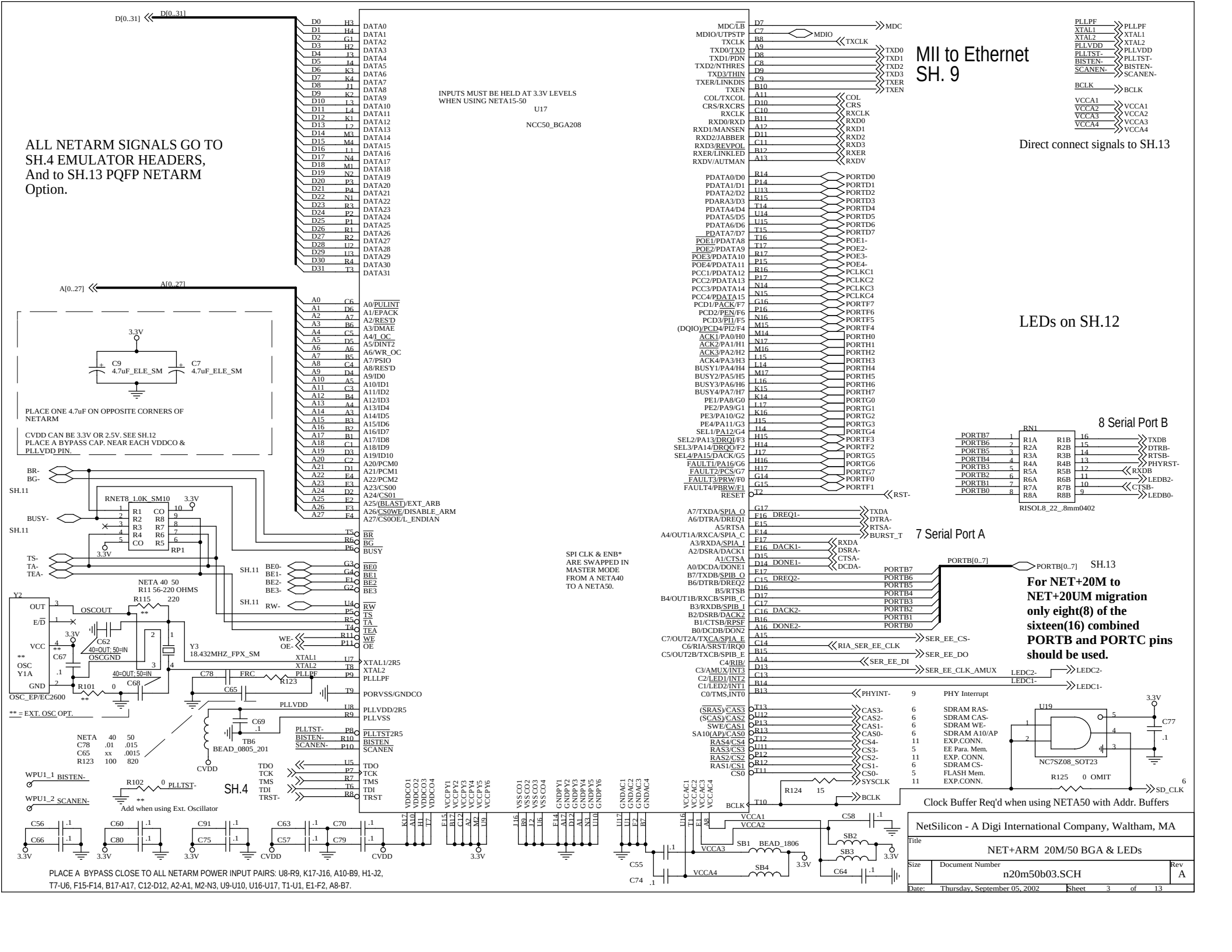
Flash Write and Read are separately controlled by dipswitch

Larger SDRAM Support can be done on Daughter Board. CS1 can be disabled on board.

ENI Port (NET+50 Only)

All Supported GPIO's go to ENI Connector
Supports ENI mode (Data Buffer if required, can be added on daughter board)

NetSilicon - A Digi International Company, Waltham, MA		
Title: NET+ARM 20M/50 Port & Chip Select Information		
Size: B	Document Number: n20m50b02.SCH	Rev: B
Date: Thursday, September 05, 2002	Sheet 2 of 13	


ALL NETARM SIGNALS GO TO SH.4 EMULATOR HEADERS, And to SH.13 PQFP NETARM Option.
INPUTS MUST BE HELD AT 3.3V LEVELS WHEN USING NETA15-50
U17
NCC50_BGA208
MII to Ethernet SH. 9
Direct connect signals to SH.13
LEDs on SH.12
8 Serial Port B
7 Serial Port A
SPI CLK & ENB* ARE SWAPPED IN MASTER MODE FROM A NETA40 TO A NETA50.
For NET+20M to NET+20UM migration only eight(8) of the sixteen(16) combined PORTB and PORTC pins should be used.
PLACE ONE 4.7uF ON OPPOSITE CORNERS OF NETARM
CVDD CAN BE 3.3V OR 2.5V. SEE SH.12
PLACE A BYPASS CAP. NEAR EACH VDDCO & PLLVDD PIN.
NETA 40 50
R11 56-220 OHMS
** = EXT. OSC OPT.
Add when using Ext. Oscillator
Clock Buffer Req'd when using NETA50 with Addr. Buffers
PLACE A BYPASS CLOSE TO ALL NETARM POWER INPUT PAIRS: U8-R9, K17-J16, A10-B9, H1-J2, T7-U6, F15-F14, B17-A17, C12-D12, A2-A1, M2-N3, U9-U10, U16-U17, T1-U1, E1-F2, A8-B7.
NetSilicon - A Digi International Company, Waltham, MA
NET+ARM 20M/50 BGA & LEDs
n20m50b03.SCH
Rev A
Thursday, September 05, 2002
Sheet 3 of 13

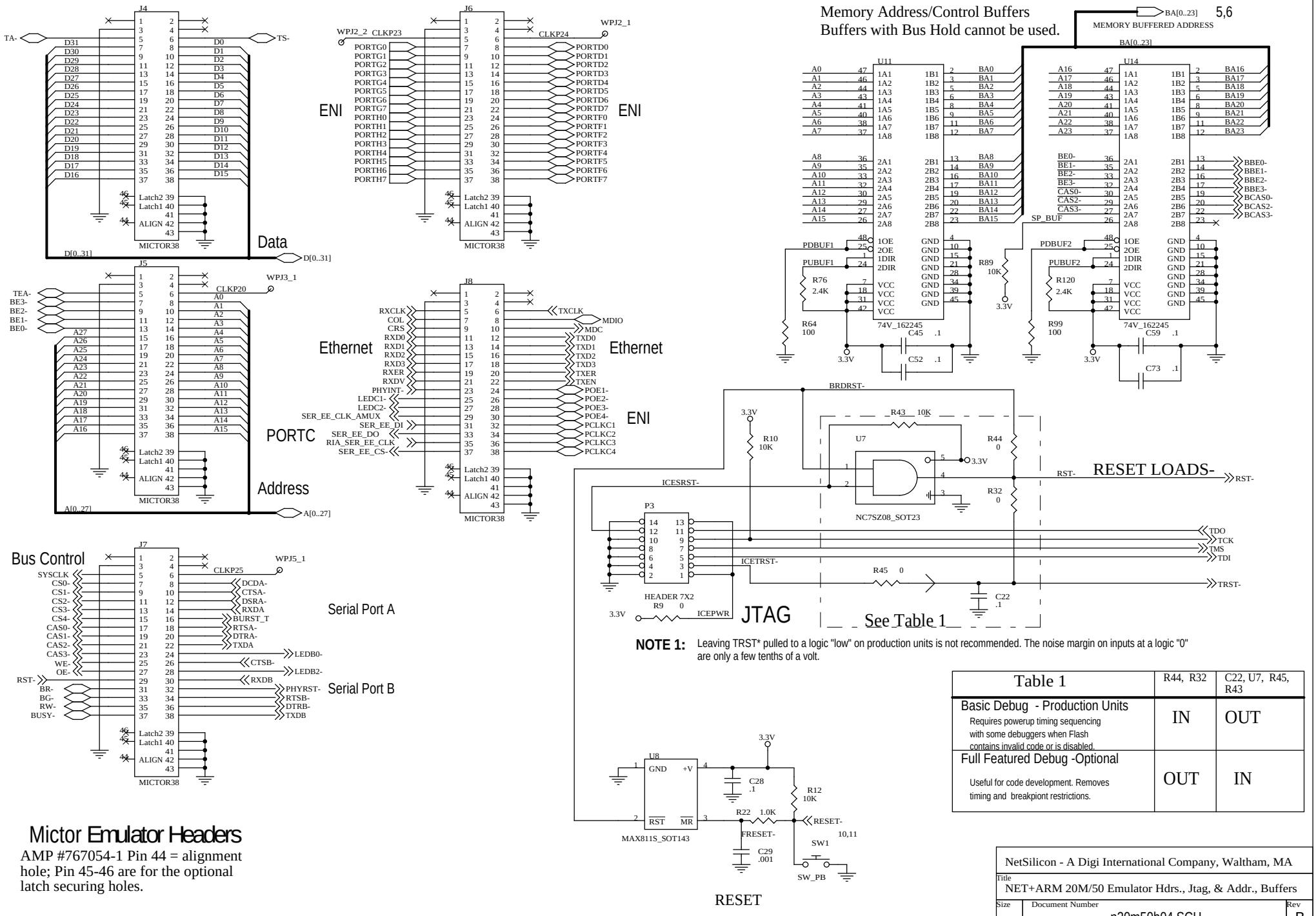


Table 1	R44, R32	C22, U7, R45, R43
Basic Debug - Production Units Requires powerup timing sequencing with some debuggers when Flash contains invalid code or is disabled.	IN	OUT
Full Featured Debug -Optional Useful for code development. Removes timing and breakpiont restrictions.	OUT	IN

Mictor Emulator Headers

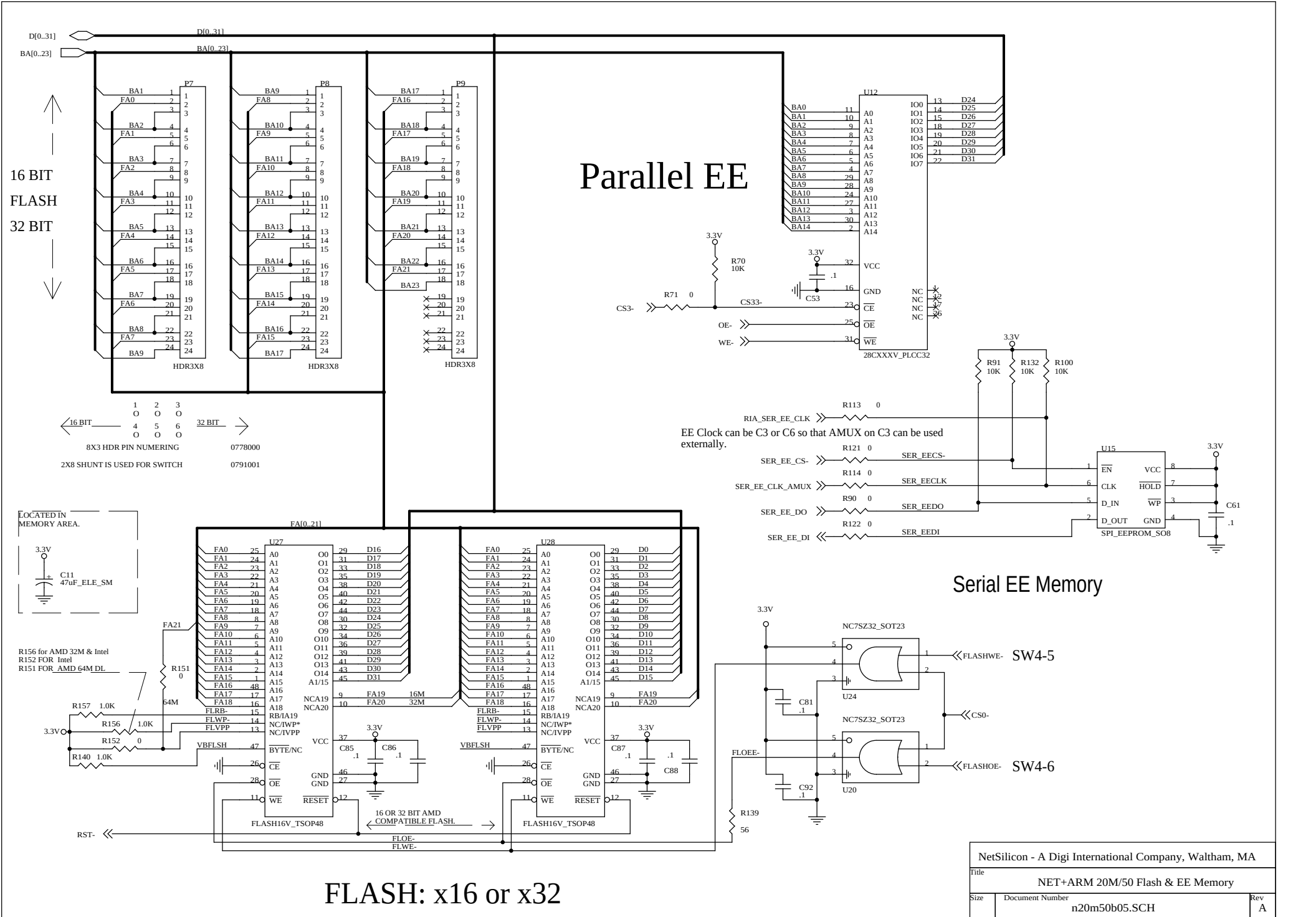
AMP #767054-1 Pin 44 = alignment hole; Pin 45-46 are for the optional latch securing holes.

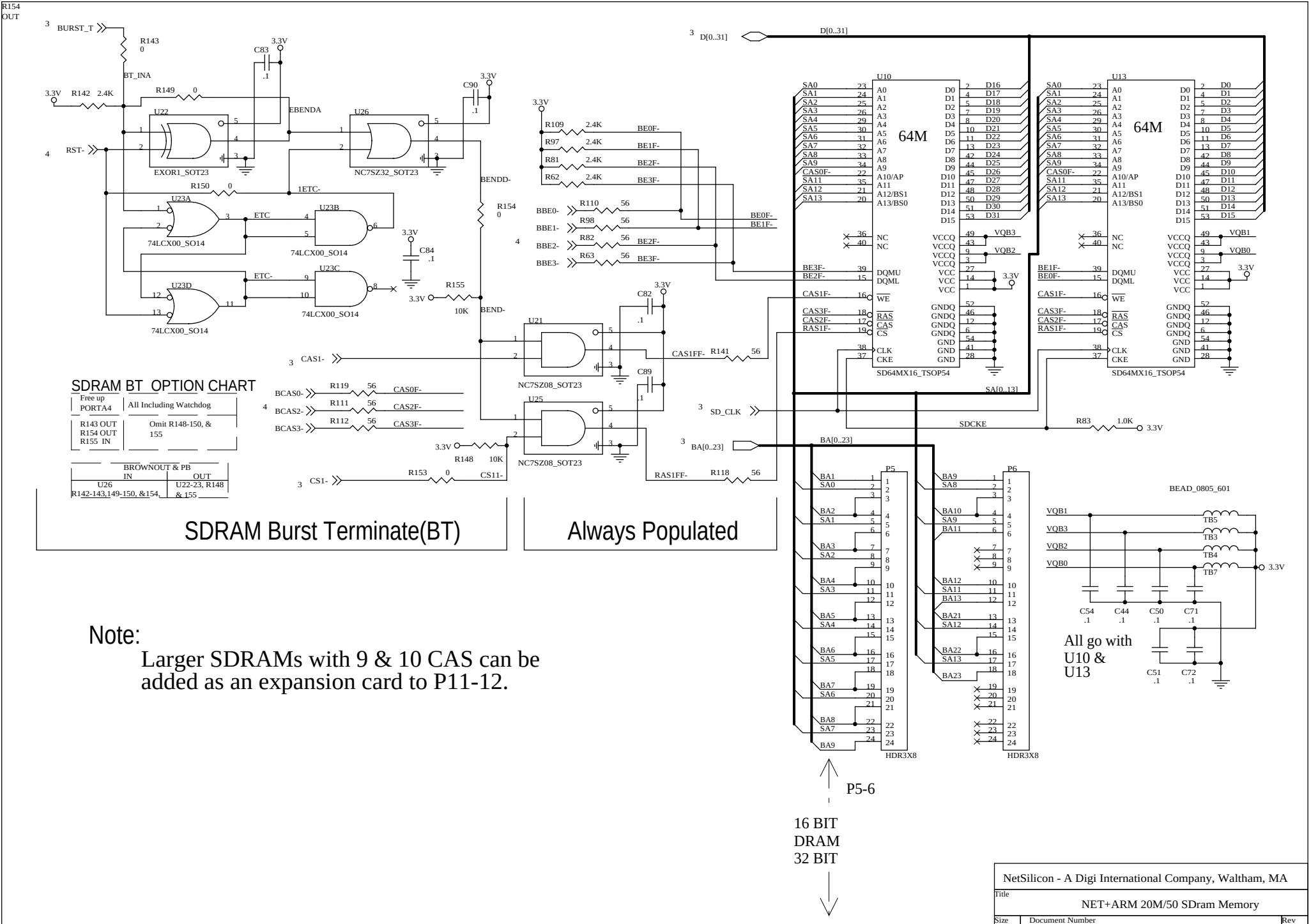
NetSilicon - A Digi International Company, Waltham, MA

Title: NET+ARM 20M/50 Emulator Hdrs., Jtag, & Addr., Buffers

Size	Document Number	Rev
	n20m50b04.SCH	B

Date: Thursday, September 05, 2002 Sheet 4 of 13


D[0..31]
BA[0..23]
16 BIT
FLASH
32 BIT
P7
P8
P9
HDR3X8
16 BIT
32 BIT
8X3 HDR PIN NUMERING
0778000
2X8 SHUNT IS USED FOR SWITCH
0791001
Parallel EE
U12
28CXXXV_PLCC32
R70
10K
R71 0
CS3-
CS33-
OE-
WE-
C53
3.3V
R91
10K
R132
10K
R100
10K
R113 0
RIA_SER_EE_CLK
EE Clock can be C3 or C6 so that AMUX on C3 can be used externally.
R121 0
SER_EE_CS-
SER_EECS-
R114 0
SER_EE_CLK_AMUX
SER_EECLK
R90 0
SER_EE_DO
SER_EEDO
R122 0
SER_EE_DI
SER_EEDI
U15
SPI_EEPROM_SO8
C61
.1
Serial EE Memory
LOCATED IN
MEMORY AREA.
C11
47uF_ELE_SM
FA[0..21]
U27
U28
FLASH16V_TSOP48
R156 for AMD 32M & Intel
R152 FOR Intel
R151 FOR AMD 64M DL
R151
0
64M
R157 1.0K
R156 1.0K
R152 0
R140 1.0K
VBFLSH
C85
C86
C87
C88
.1
16M
32M
16 OR 32 BIT AMD
COMPATIBLE FLASH.
RST-
FLOE-
FLWE-
NC7SZ32_SOT23
U24
U20
C81
C92
FLASHWE-
FLASHOE-
CS0-
FLOEE-
SW4-5
SW4-6
R139
56
FLASH: x16 or x32
NetSilicon - A Digi International Company, Waltham, MA
Title
NET+ARM 20M/50 Flash & EE Memory
Size
Document Number
n20m50b05.SCH
Rev
A
Date: Thursday, September 05, 2002
Sheet 5 of 13



SDRAM BT OPTION CHART

Free up PORTA4	All Including Watchdog
R143 OUT R154 OUT R155 IN	Omit R148-150, & 155

BROWNOUT & PB	
IN	OUT
U26	U22-23, R148 & 155
R142-143,149-150, &154	

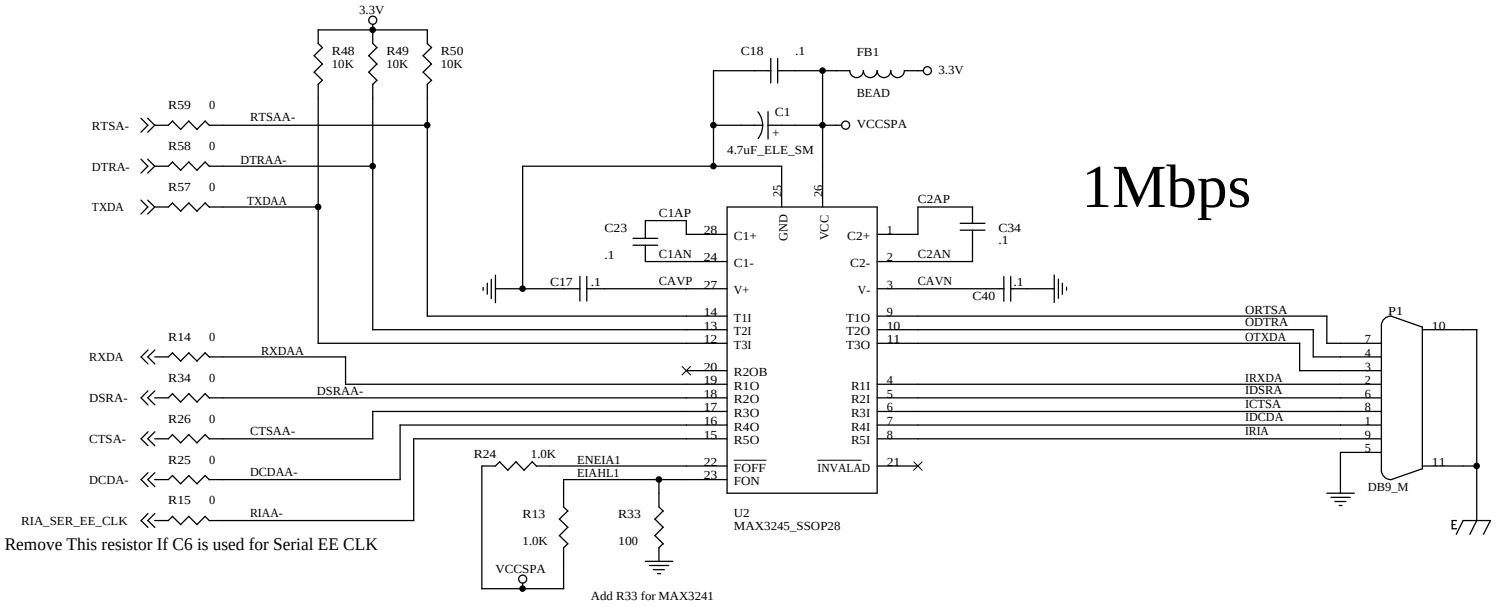
SDRAM Burst Terminate(BT)

Always Populated

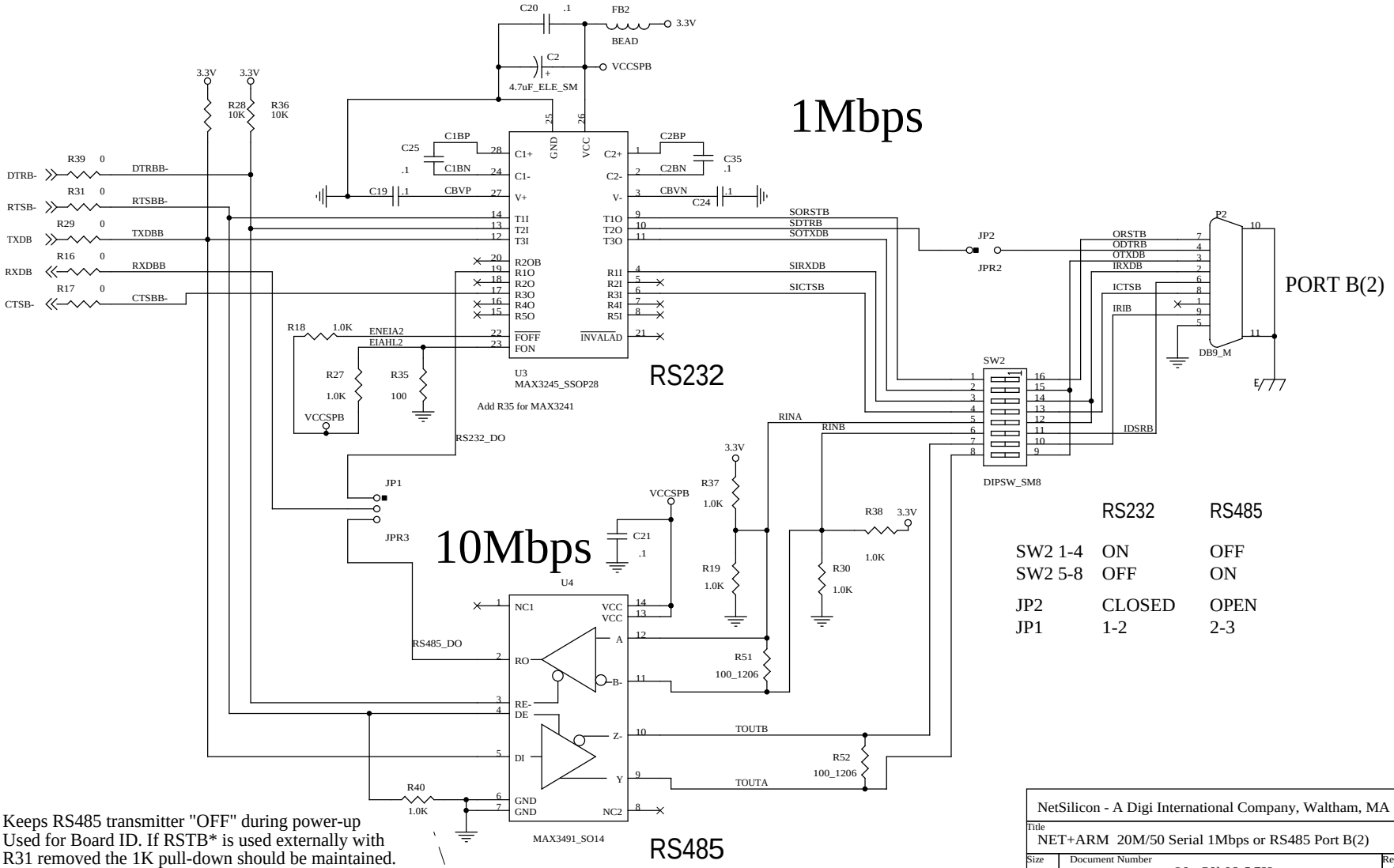
Note:

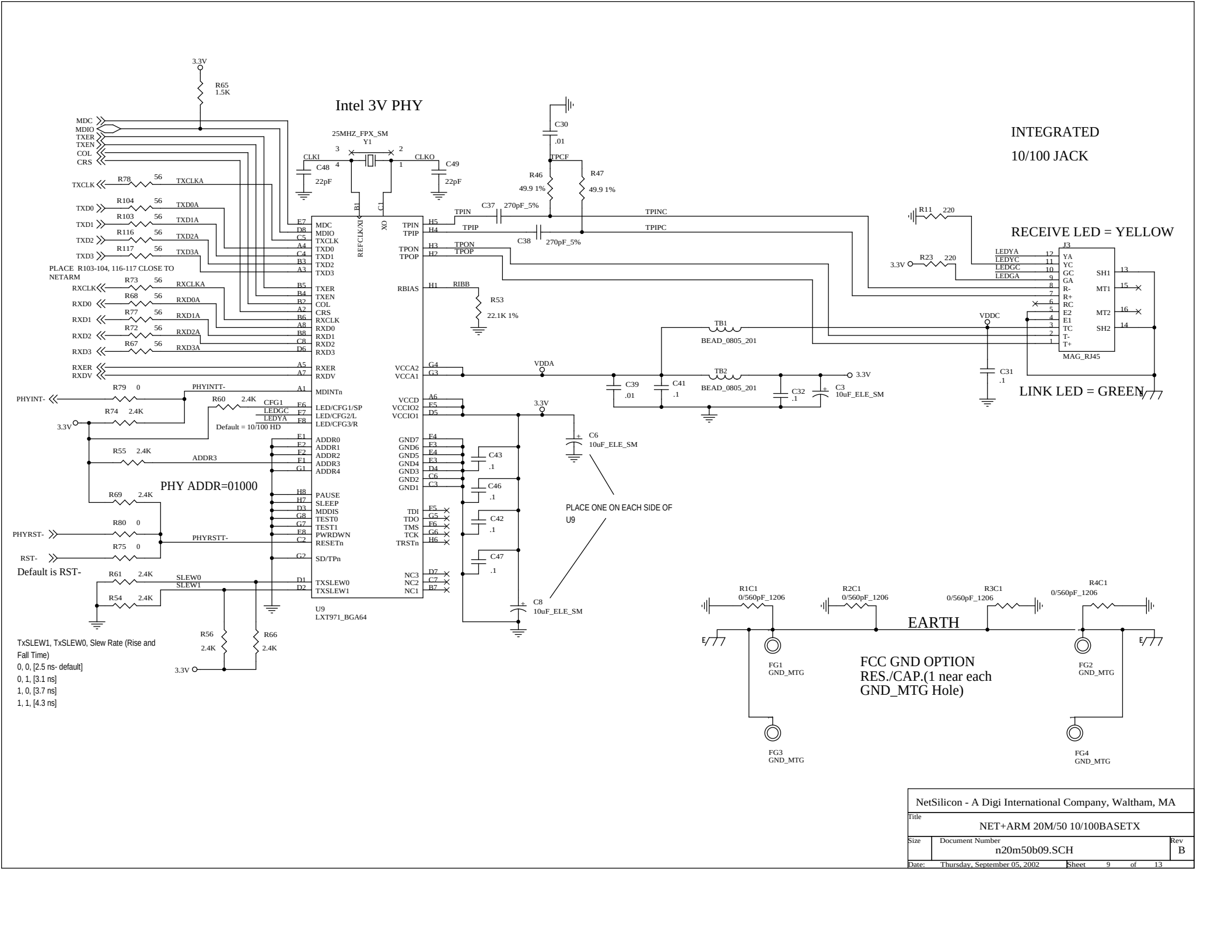
Larger SDRAMs with 9 & 10 CAS can be added as an expansion card to P11-12.

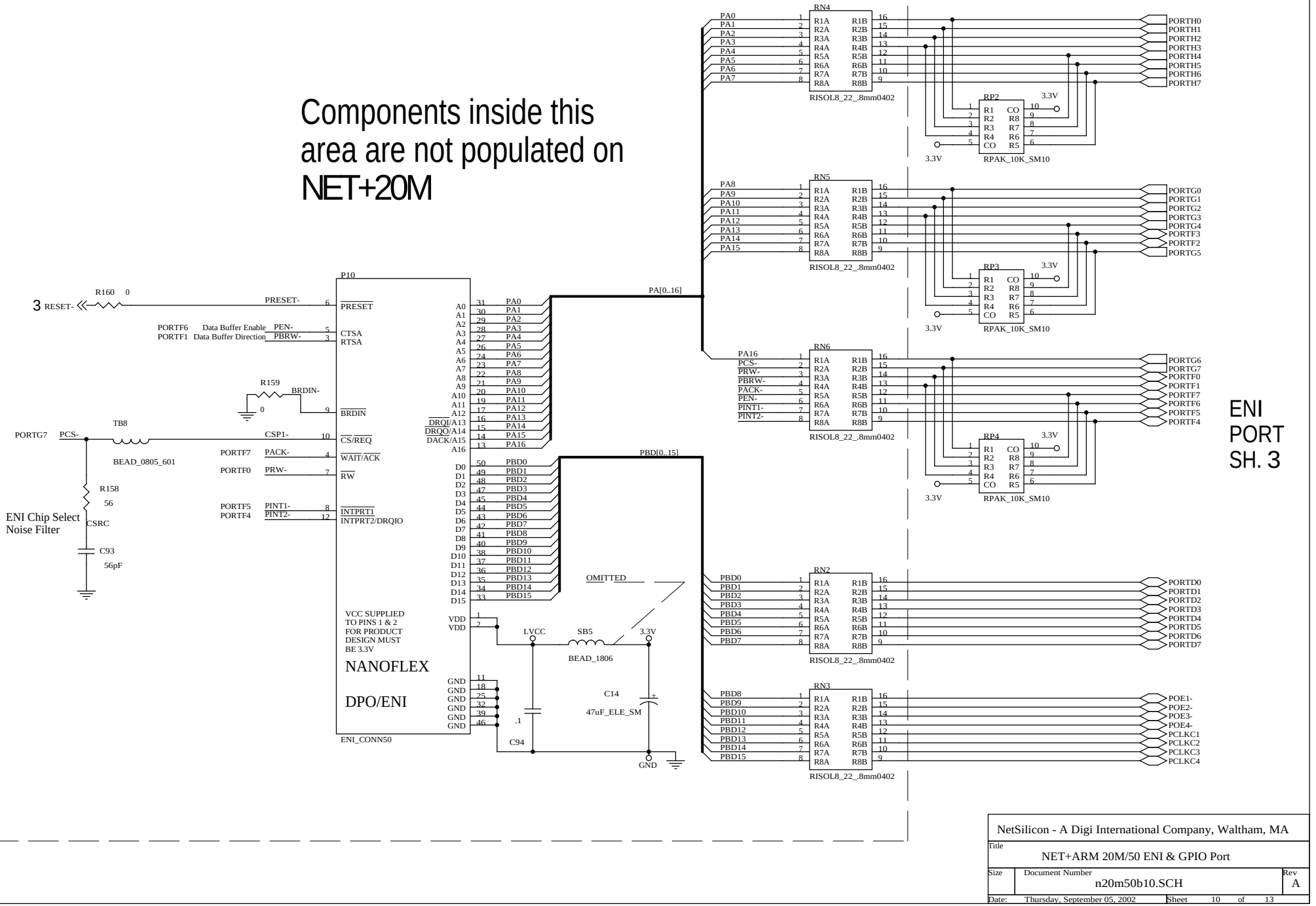
NetSilicon - A Digi International Company, Waltham, MA		
Title: NET+ARM 20M/50 SDram Memory		
Size	Document Number: n20m50b06.SCH	Rev: A
Date: Thursday, September 05, 2002	Sheet 6 of 13	



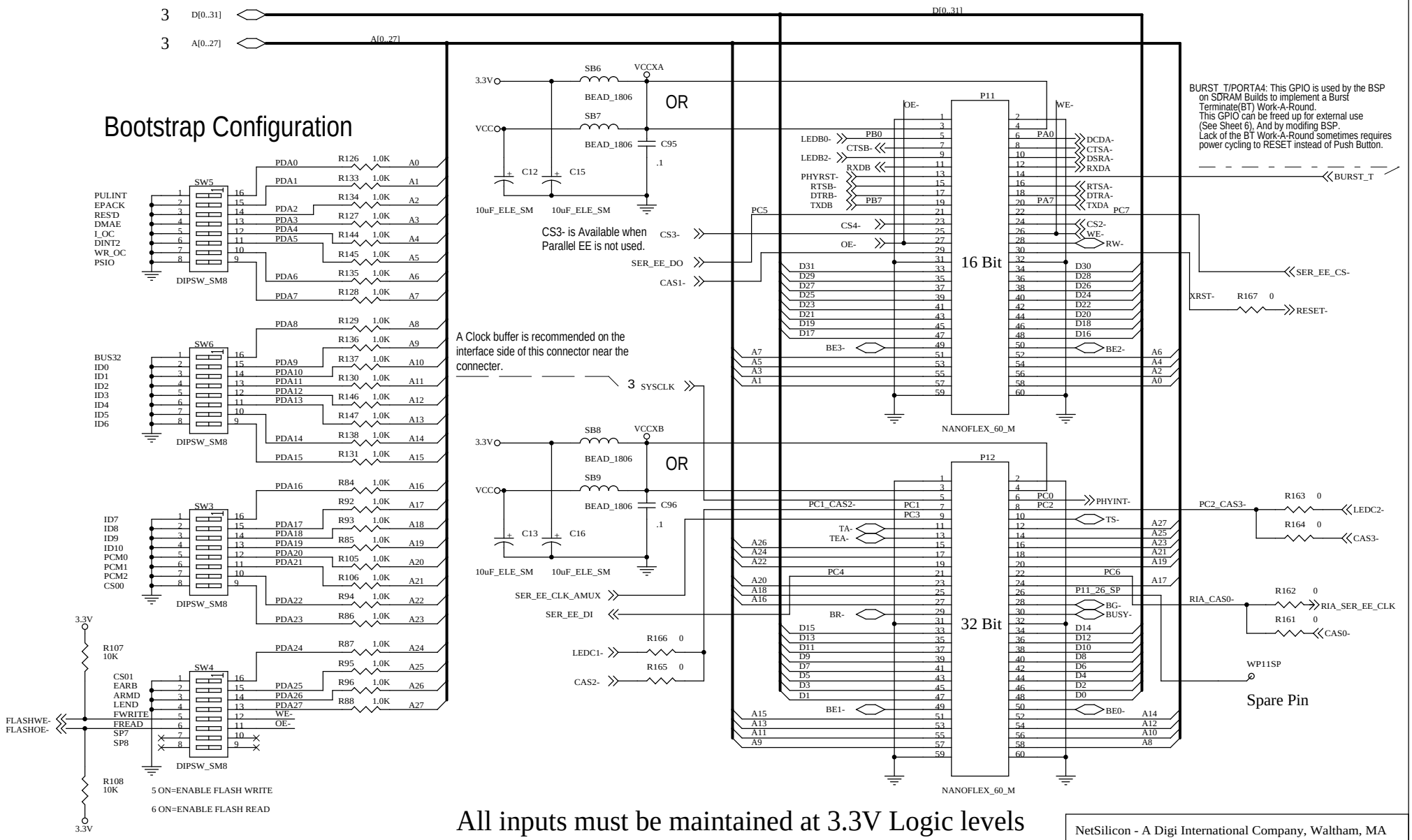
NetSilicon - A Digi International Company, Waltham, MA		
Title: NET+ARM 20M/50 Serial 1Mbps		
Size	Document Number: n20m50b07.SCH	Rev: A
Date: Thursday, September 05, 2002	Sheet 7 of 13	


1Mbps
10Mbps
RS232
RS485
PORT B(2)
U3
MAX3245_SSOP28
Add R35 for MAX3241
U4
MAX3491_SO14
DIPSW_SM8
DB9_M
JPR2
JPR3
C20 .1
FB2
BEAD
3.3V
C2
4.7uF_ELE_SM
VCCSPB
R28 10K
R36 10K
C25 .1
C35 .1
C19 .1
C24 .1
C1BP
C1BN
CBVP
C2BP
C2BN
CBVN
DTRB-
RTSB-
TXDB
RXDB
CTSB-
DTRBB-
RTSBB-
TXDBB
RXDBB
CTSBB-
R39 0
R31 0
R29 0
R16 0
R17 0
SORSTB
SDTRB
SOTXDB
SIRXDB
SICTSB
ORSTB
ODTRB
OTXDB
IRXDB
ICTSB
IRIB
IDSRB
R18 1.0K
ENEIA2
EIAHL2
R27 1.0K
R35 100
RS232_DO
RS485_DO
RINA
RINB
R37 1.0K
R38 1.0K
R19 1.0K
R30 1.0K
R51 100_1206
R52 100_1206
TOUTB
TOUTA
R40 1.0K
C21 .1
SW2
JP1
JP2
RS232 RS485
SW2 1-4 ON OFF
SW2 5-8 OFF ON
JP2 CLOSED OPEN
JP1 1-2 2-3
Keeps RS485 transmitter "OFF" during power-up
Used for Board ID. If RSTB* is used externally with
R31 removed the 1K pull-down should be maintained.
NetSilicon - A Digi International Company, Waltham, MA
Title
NET+ARM 20M/50 Serial 1Mbps or RS485 Port B(2)
Size
Document Number
n20m50b08.SCH
Rev
B
Date: Thursday, September 05, 2002
Sheet 8 of 13


Intel 3V PHY
INTEGRATED
10/100 JACK
RECEIVE LED = YELLOW
LINK LED = GREEN
PHY ADDR=01000
PLACE R103-104, 116-117 CLOSE TO NETARM
PLACE ONE ON EACH SIDE OF U9
Default is RST-
Default = 10/100 HD
U9
LXT971_BGA64
MAG_RJ45
EARTH
FCC GND OPTION
RES./CAP.(1 near each GND_MTG Hole)
TxSLEW1, TxSLEW0, Slew Rate (Rise and Fall Time)
0, 0, [2.5 ns- default]
0, 1, [3.1 ns]
1, 0, [3.7 ns]
1, 1, [4.3 ns]
NetSilicon - A Digi International Company, Waltham, MA
NET+ARM 20M/50 10/100BASETX
n20m50b09.SCH
B
Thursday, September 05, 2002
Sheet 9 of 13


Components inside this area are not populated on NET+20M
ENI PORT SH. 3
P10
ENI_CONN50
NANOFLEX
DPO/ENI
VCC SUPPLIED TO PINS 1 & 2 FOR PRODUCT DESIGN MUST BE 3.3V
OMITTED
ENI Chip Select Noise Filter
RESET-
PRESET-
PORTF6 Data Buffer Enable PEN-
PORTF1 Data Buffer Direction PBRW-
BRDIN-
PCS-
CSP1-
PORTF7 PACK-
PORTF0 PRW-
PORTF5 PINT1-
PORTF4 PINT2-
BEAD_0805_601
BEAD_1806
47uF_ELE_SM
PA[0..16]
PBD[0..15]
RISOL8_22_.8mm0402
RPAK_10K_SM10
NetSilicon - A Digi International Company, Waltham, MA
Title
NET+ARM 20M/50 ENI & GPIO Port
Size
Document Number
n20m50b10.SCH
Rev
A
Date: Thursday, September 05, 2002
Sheet 10 of 13

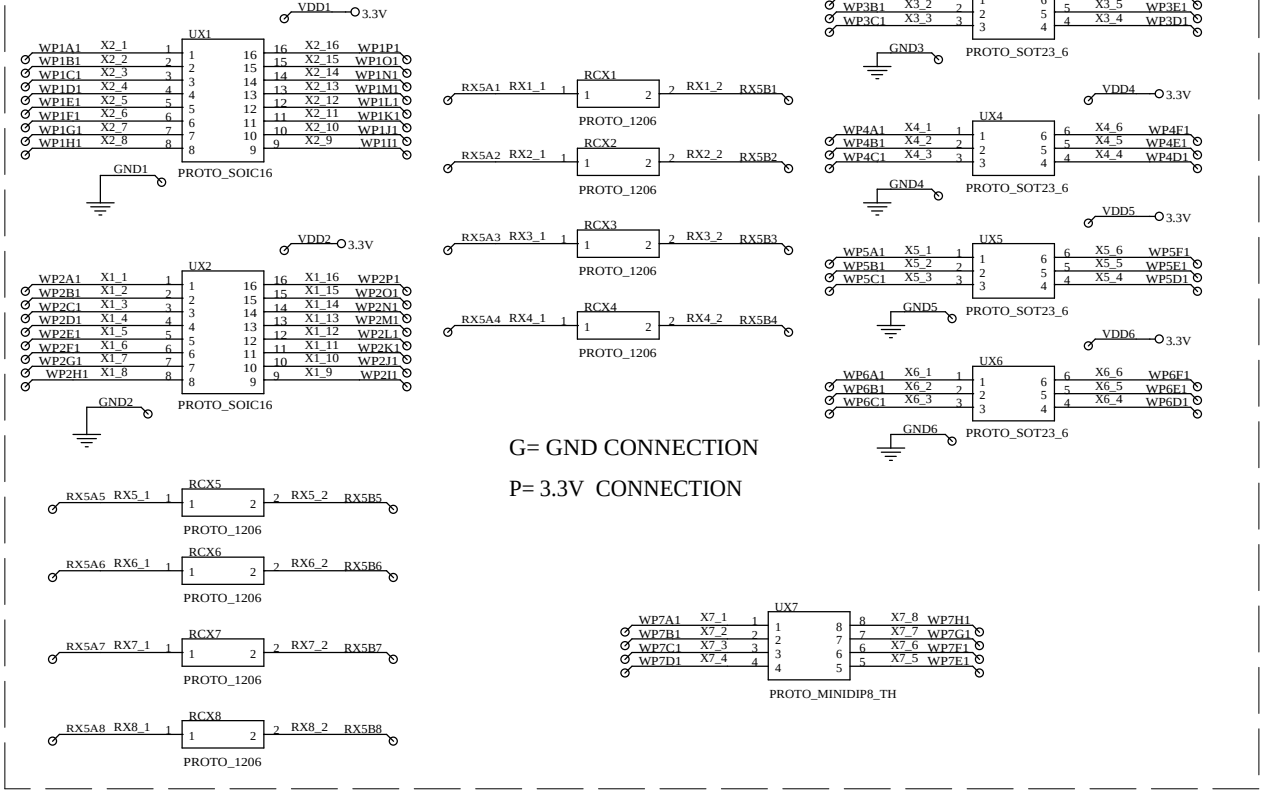
Expansion Connectors

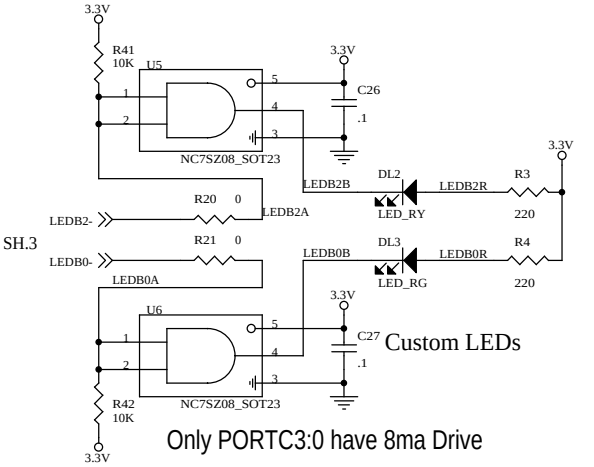


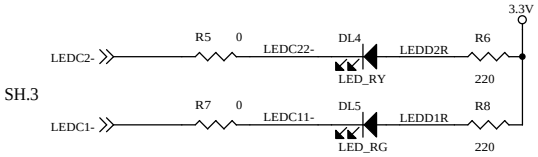
All inputs must be maintained at 3.3V Logic levels

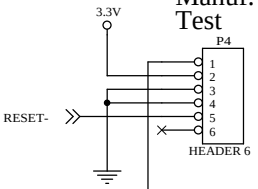
NetSilicon - A Digi International Company, Waltham, MA		
Title: NET+ARM 20M/50 Expansion & Dipswitches		
Size	Document Number: n20m50b11.SCH	Rev: A
Date: Thursday, September 05, 2002	Sheet 11 of 13	

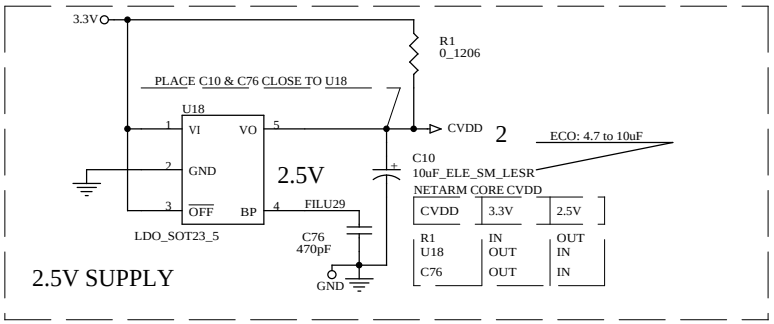
Prototyping Area

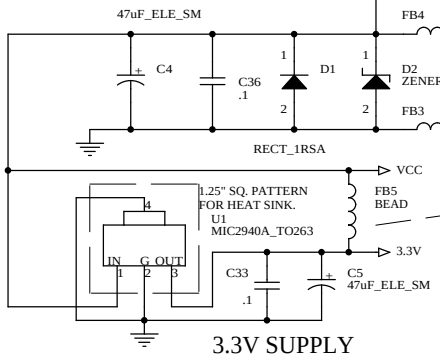


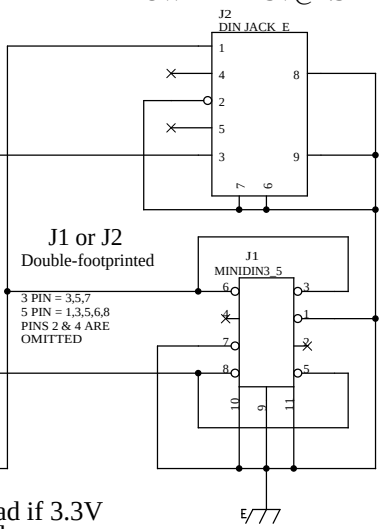




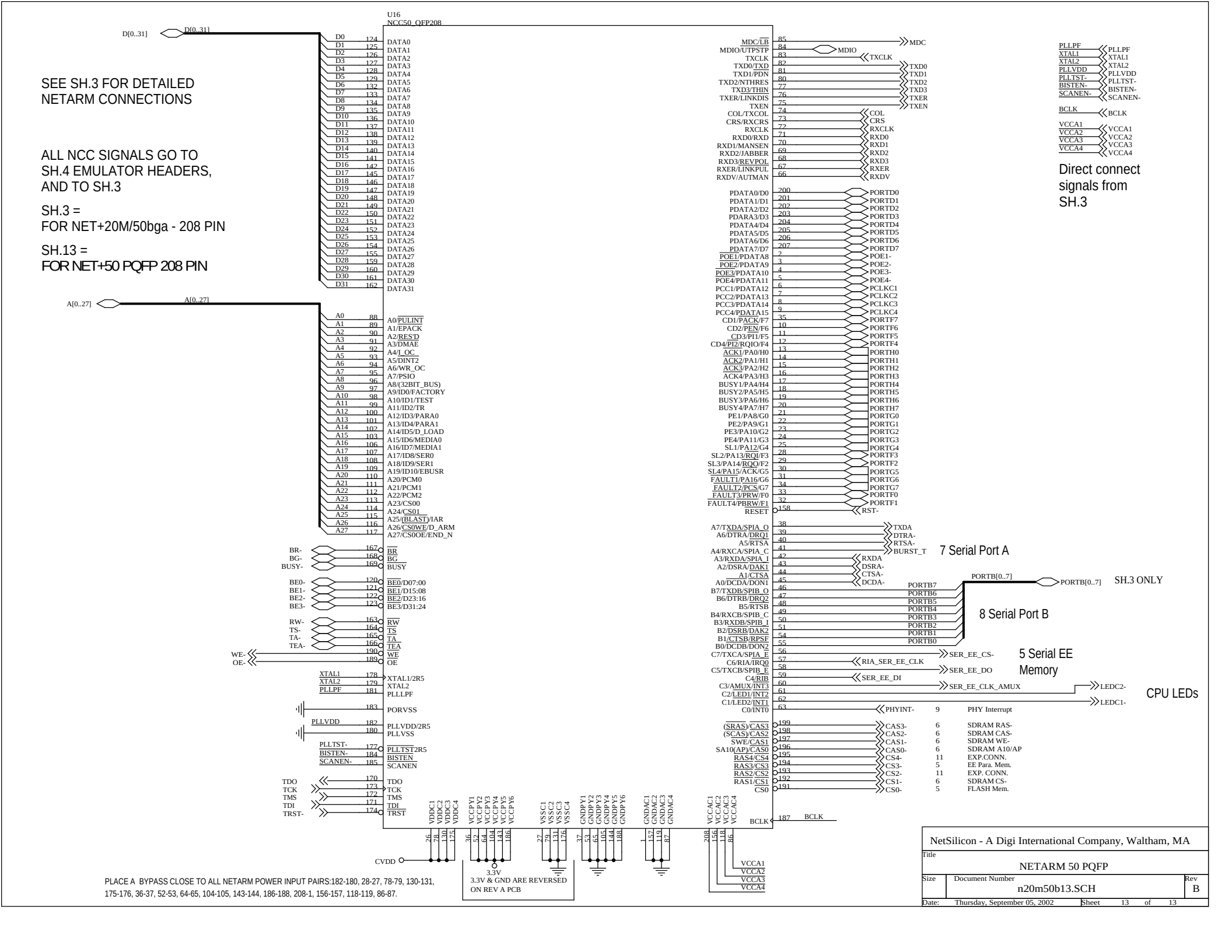








NetSilicon - A Digi International Company, Waltham, MA		
Title: NET+ARM Power Supply, & Breadboard Area		
Size	Document Number: n20m50b12.SCH	Rev: B
Date: Thursday, September 05, 2002	Sheet 12 of 13	


U16
NCC50_QFP208
SEE SH.3 FOR DETAILED NETARM CONNECTIONS
ALL NCC SIGNALS GO TO SH.4 EMULATOR HEADERS, AND TO SH.3
SH.3 = FOR NET+20M/50bga - 208 PIN
SH.13 = FOR NET+50 PQFP 208 PIN
D[0..31]
A[0..27]
DATA0
DATA1
DATA2
DATA3
DATA4
DATA5
DATA6
DATA7
DATA8
DATA9
DATA10
DATA11
DATA12
DATA13
DATA14
DATA15
DATA16
DATA17
DATA18
DATA19
DATA20
DATA21
DATA22
DATA23
DATA24
DATA25
DATA26
DATA27
DATA28
DATA29
DATA30
DATA31
A0/PULINT
A1/EPACK
A2/RESTD
A3/DMAE
A4/I_OC
A5/DINT2
A6/WR_OC
A7/PSIO
A8/(32BIT_BUS)
A9/ID0/FACTORY
A10/ID1/TEST
A11/ID2/TR
A12/ID3/PARA0
A13/ID4/PARA1
A14/ID5/D_LOAD
A15/ID6/MEDIA0
A16/ID7/MEDIA1
A17/ID8/SER0
A18/ID9/SER1
A19/ID10/EBUSR
A20/PCM0
A21/PCM1
A22/PCM2
A23/CS00
A24/CS01
A25/(BLAST)/IAR
A26/CS0WE/D_ARM
A27/CS0OE/END_N
BR-
BG-
BUSY-
BE0-
BE1-
BE2-
BE3-
RW-
TS-
TA-
TEA-
WE-
OE-
BE0/D07:00
BE1/D15:08
BE2/D23:16
BE3/D31:24
XTAL1
XTAL2
PLLPF
PLLVDD
PLLTST-
BISTEN-
SCANEN-
XTAL1/2R5
XTAL2
PLLPF
PORVSS
PLLVDD/2R5
PLLVSS
PLLTST2R5
BISTEN
SCANEN
TDO
TCK
TMS
TDI
TRST-
MDC/LB
MDIO/UTPSTP
TXCLK
TXD0/TXD
TXD1/PDN
TXD2/NTHRES
TXD3/THIN
TXER/LINKDIS
TXEN
COL/TXCOL
CRS/RXCRS
RXCLK
RXD0/RXD
RXD1/MANSEN
RXD2/JABBER
RXD3/REVPOL
RXER/LINKPUL
RXDV/AUTMAN
MDC
MDIO
TXCLK
TXD0
TXD1
TXD2
TXD3
TXER
TXEN
COL
CRS
RXCLK
RXD0
RXD1
RXD2
RXD3
RXER
RXDV
PDATA0/D0
PDATA1/D1
PDATA2/D2
PDARA3/D3
PDATA4/D4
PDATA5/D5
PDATA6/D6
PDATA7/D7
POE1/PDATA8
POE2/PDATA9
POE3/PDATA10
POE4/PDATA11
PCC1/PDATA12
PCC2/PDATA13
PCC3/PDATA14
PCC4/PDATA15
CD1/PACK/F7
CD2/PEN/F6
CD3/PI1/F5
CD4/PI2/RQIO/F4
ACK1/PA0/H0
ACK2/PA1/H1
ACK3/PA2/H2
ACK4/PA3/H3
BUSY1/PA4/H4
BUSY2/PA5/H5
BUSY3/PA6/H6
BUSY4/PA7/H7
PE1/PA8/G0
PE2/PA9/G1
PE3/PA10/G2
PE4/PA11/G3
SL1/PA12/G4
SL2/PA13/RQI/F3
SL3/PA14/RQO/F2
SL4/PA15/ACK/G5
FAULT1/PA16/G6
FAULT2/PCS/G7
FAULT3/PRW/F0
FAULT4/PBRW/F1
RESET
PORTD0
PORTD1
PORTD2
PORTD3
PORTD4
PORTD5
PORTD6
PORTD7
POE1-
POE2-
POE3-
POE4-
PCLKC1
PCLKC2
PCLKC3
PCLKC4
PORTF7
PORTF6
PORTF5
PORTF4
PORTH0
PORTH1
PORTH2
PORTH3
PORTH4
PORTH5
PORTH6
PORTH7
PORTG0
PORTG1
PORTG2
PORTG3
PORTG4
PORTF3
PORTF2
PORTG5
PORTG6
PORTG7
PORTF0
PORTF1
RST-
A7/TXDA/SPIA_O
A6/DTRA/DRQ1
A5/RTSA
A4/RXCA/SPIA_C
A3/RXDA/SPIA_I
A2/DSRA/DAK1
A1/CTSA
A0/DCDA/DON1
B7/TXDB/SPIB_O
B6/DTRB/DRQ2
B5/RTSB
B4/RXCB/SPIB_C
B3/RXDB/SPIB_I
B2/DSRB/DAK2
B1/CTSB/RPSF
B0/DCDB/DON2
C7/TXCA/SPIA_E
C6/RIA/IRQ0
C5/TXCB/SPIB_E
C4/RIB
C3/AMUX/INT3
C2/LED1/INT2
C1/LED2/INT1
C0/INT0
TXDA
DTRA-
RTSA-
BURST_T
RXDA
DSRA-
CTSA-
DCDA-
7 Serial Port A
PORTB[0..7]
PORTB7
PORTB6
PORTB5
PORTB4
PORTB3
PORTB2
PORTB1
PORTB0
8 Serial Port B
SH.3 ONLY
SER_EE_CS-
SER_EE_DO
SER_EE_DI
SER_EE_CLK_AMUX
5 Serial EE Memory
RIA_SER_EE_CLK
LEDC2-
LEDC1-
CPU LEDs
PHYINT-
PHY Interrupt
(SRAS)/CAS3
(SCAS)/CAS2
SWE/CAS1
SA10(AP)/CAS0
RAS4/CS4
RAS3/CS3
RAS2/CS2
RAS1/CS1
CS0
SDRAM RAS-
SDRAM CAS-
SDRAM WE-
SDRAM A10/AP
EXP.CONN.
EE Para. Mem.
EXP. CONN.
SDRAM CS-
FLASH Mem.
BCLK
PLLPF
XTAL1
XTAL2
PLLVDD
PLLTST-
BISTEN-
SCANEN-
VCCA1
VCCA2
VCCA3
VCCA4
Direct connect signals from SH.3
VDDC1
VDDC2
VDDC3
VDDC4
VCCPY1
VCCPY2
VCCPY3
VCCPY4
VCCPY5
VCCPY6
VSSC1
VSSC2
VSSC3
VSSC4
GNDPY1
GNDPY2
GNDPY3
GNDPY4
GNDPY5
GNDPY6
GNDAC1
GNDAC2
GNDAC3
GNDAC4
VCCAC1
VCCAC2
VCCAC3
VCCAC4
CVDD
3.3V
3.3V & GND ARE REVERSED ON REV A PCB
PLACE A BYPASS CLOSE TO ALL NETARM POWER INPUT PAIRS:182-180, 28-27, 78-79, 130-131, 175-176, 36-37, 52-53, 64-65, 104-105, 143-144, 186-188, 208-1, 156-157, 118-119, 86-87.
NetSilicon - A Digi International Company, Waltham, MA
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Size
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