Pin Number	Signal Name	Pull Up/Down	OD (mA)	I/O	PCI Interface Buf Type	Description
J24	ad[0]			I/O	BDPCI	PCI time-multiplexed address/data bus
H26	ad[1]			I/O	BDPCI	.
J25	ad[2]			I/O	BDPCI	.
J26	ad[3]			I/O	BDPCI	.
K24	ad[4]			I/O	BDPCI	.
K25	ad[5]			I/O	BDPCI	.
K26	ad[6]			I/O	BDPCI	.
L24	ad[7]			I/O	BDPCI	.
L26	ad[8]			I/O	BDPCI	.
M24	ad[9]			I/O	BDPCI	.
M25	ad[10]			I/O	BDPCI	.
M26	ad[11]			I/O	BDPCI	.
N24	ad[12]			I/O	BDPCI	.
N25	ad[13]			I/O	BDPCI	.
N26	ad[14]			I/O	BDPCI	.
P26	ad[15]			I/O	BDPCI	.
U24	ad[16]			I/O	BDPCI	.
V26	ad[17]			I/O	BDPCI	.
V25	ad[18]			I/O	BDPCI	.
W26	ad[19]			I/O	BDPCI	.
V24	ad[20]			I/O	BDPCI	.
W25	ad[21]			I/O	BDPCI	.
Y26	ad[22]			I/O	BDPCI	.
W24	ad[23]			I/O	BDPCI	.
Y24	ad[24]			I/O	BDPCI	.
AA25	ad[25]			I/O	BDPCI	.
AB26	ad[26]			I/O	BDPCI	.
AA24	ad[27]			I/O	BDPCI	.
AB25	ad[28]			I/O	BDPCI	.
AC26	ad[29]			I/O	BDPCI	.
AD26	ad[30]			I/O	BDPCI	.
AC25	ad[31]			I/O	BDPCI	.
L25	cbe_n[0]			I/O	BDPCI	command/byte enables
P25	cbe_n[1]			I/O	BDPCI	.
U25	cbe_n[2]			I/O	BDPCI	.
AA26	cbe_n[3]			I/O	BDPCI	.
T26	devsel_n			I/O	BDPCI	device select
U26	frame_n			I/O	BDPCI	cycle frame
Y25	idsel			I	IPCI	initialization device select
T24	irdy_n			I/O	BDPCI	initiator ready
P24	par			I/O	BDPCI	parity signal
R25	perr_n			I/O	BDPCI	parity error
R26	serr_n			I/O	BDPCI	system error
R24	stop_n			I/O	BDPCI	stop signal
T25	trdy_n			I/O	BDPCI	target ready
AC24	pci_arb_gnt_1_n			O	BTPCI	PCI channel 1 grant
AD23	pci_arb_gnt_2_n			O	BTPCI	PCI channel 2 grant
AE24	pci_arb_gnt_3_n			O	BTPCI	PCI channel 3 grant
AD25	pci_arb_req_1_n			I	IPCI	PCI channel 1 request
AB23	pci_arb_req_2_n			I	IPCI	PCI channel 2 request

AC22	pci_arb_req_3_n			I	IPCI	PCI channel 3 request
AF23	pci_central_resource_n	pull down		I	IBUFDIF	PCI internal central resource enable
AF25	pci_int_a_n			I/O	BDPCI	PCI interrupt request a, output if external central resource used
AF24	pci_int_b_n			I/O	BDPCI	PCI interrupt request b, CCLKRUN# for Cardbus applications
AE23	pci_int_c_n			I	IPCI	PCI interrupt request c
AD22	pci_int_d_n			I	IPCI	PCI interrupt request d
AE26	pci_reset_n			I/O	BDPCI	PCI reset, output if internal central resource enabled
AB24	pci_clk_in	pull up		I	IPCIU	PCI clock in
AA23	pci_clk_out			O	BTPCI	PCI clock out

Multifunction GPIO

Pin Number	Signal Name		OD (mA)	I/O	Buf Type	Descriptions (four options)
AF19	gpio[0]	pull up	2	I/O	BD2CUIF	Ser port A TxData / DMA ch 0 done / Timer 1 / GPIO 0
AE18	gpio[1]	pull up	2	I/O	BD2CUIF	Ser port A RxData / DMA ch 0 req / Ext IRQ 0 / GPIO 1
AF18	gpio[2]	pull up	2	I/O	BD2CUIF	Ser port A RTS / Timer 0 / DMA ch 1 ack / GPIO 2
AD17	gpio[3]	pull up	2	I/O	BD2CUIF	Ser port A CTS / 1284 periph ack / DMA ch 0 req / GPIO 3
AE17	gpio[4]	pull up	2	I/O	BD2CUIF	Ser port A DTR / 1284 periph busy / DMA ch 0 done / GPIO 4
AF17	gpio[5]	pull up	2	I/O	BD2CUIF	Ser port A DSR / 1284 periph error / DMA ch 0 ack / GPIO 5
AD16	gpio[6]	pull up	2	I/O	BD2CUIF	Ser port A RxClk / 1284 paper jam / Timer 7 / GPIO 6
AE16	gpio[7]	pull up	2	I/O	BD2CUIF	Ser port A TxClk / DMA ch 0 ack / Ext IRQ 1 / GPIO 7
AD15	gpio[8]	pull up	2	I/O	BD2CUIF	Ser port B TxData / reserved / reserved / GPIO 8
AE15	gpio[9]	pull up	2	I/O	BD2CUIF	Ser port B RxData / reserved / Timer 8 / GPIO 9
AF15	gpio[10]	pull up	2	I/O	BD2CUIF	Ser port B RTS / reserved / reserved / GPIO 10
AD14	gpio[11]	pull up	2	I/O	BD2CUIF	Ser port B CTS / reserved / Timer 0 / GPIO 11
AE14	gpio[12]	pull up	2	I/O	BD2CUIF	Ser port B DTR / reserved / reserved / GPIO 12
AF14	gpio[13]	pull up	2	I/O	BD2CUIF	Ser port B DSR / Ext IRQ 0 / Timer 10 / GPIO 13
AF13	gpio[14]	pull up	2	I/O	BD2CUIF	Ser port B RxClk / Timer 1 / reserved / GPIO 14
AE13	gpio[15]	pull up	2	I/O	BD2CUIF	Ser port B TxClk / Timer 2 / reserved / GPIO 15
AD13	gpio[16]	pull up	2	I/O	BD2CUIF	USB overcurrent / 1284 paper jam / Timer 11 / GPIO 16
AF12	gpio[17]	pull up	2	I/O	BD2CUIF	USB power relay / reserved / reserved / GPIO 17
AE12	gpio[18]	pull up	4	I/O	BD4CUIF	Ethernet CAM reject / LCD power enable / Ext IRQ 3 / GPIO 18
AD12	gpio[19]	pull up	4	I/O	BD4CUIF	Ethernet CAM Req / LCD line-horz sync / DMA ch 1 ack / GPIO 19
AC12	gpio[20]	pull up	8	I/O	BD8CUIF	Ser port C DTR / LCD clock / reserved / GPIO 20
AF11	gpio[21]	pull up	4	I/O	BD4CUIF	Ser port C DSR / LCD frame pulse-vert / reserved / GPIO 21
AE11	gpio[22]	pull up	4	I/O	BD4CUIF	Ser port C RxClk / LCD AC bias - data enable / reserved / GPIO 22
AD11	gpio[23]	pull up	4	I/O	BD4CUIF	Ser port C TxClk / LCD line end / Timer 14 / GPIO 23
AF10	gpio[24]	pull up	4	I/O	BD4CUIF	Ser port D DTR / LCD data bit 0 / reserved / GPIO 24
AE10	gpio[25]	pull up	4	I/O	BD4CUIF	Ser port D DSR / LCD data bit 1 / Timer 15 / GPIO 25
AD10	gpio[26]	pull up	4	I/O	BD4CUIF	Ser port D RxClk / LCD data bit 2 / Timer 3 / GPIO 26
AF9	gpio[27]	pull up	4	I/O	BD4CUIF	Ser port D TxClk / LCD data bit 3 / Timer 4 / GPIO 27
AE9	gpio[28]	pull up	4	I/O	BD4CUIF	Ext IRQ 1 / LCD data bit 4 / LCD data bit 8 / GPIO 28
AF8	gpio[29]	pull up	4	I/O	BD4CUIF	Timer 5 / LCD data bit 5 / LCD data bit 9 / GPIO 29
AD9	gpio[30]	pull up	4	I/O	BD4CUIF	Timer 6 / LCD data bit 6 / LCD data bit 10 / GPIO 30
AE8	gpio[31]	pull up	4	I/O	BD4CUIF	Timer 7 / LCD data bit 7 / LCD data bit 11 / GPIO 31
AF7	gpio[32]	pull up	4	I/O	BD4CUIF	Ext IRQ 2 / 1284 data bit 0 / LCD data bit 8 / GPIO 32
AD8	gpio[33]	pull up	4	I/O	BD4CUIF	Timer 8 / 1284 data bit 1 / LCD data bit 9 / GPIO 33
AD7	gpio[34]	pull up	4	I/O	BD4CUIF	Timer 9 / 1284 data bit 2 / LCD data bit 10 / GPIO 34
AE6	gpio[35]	pull up	4	I/O	BD4CUIF	Timer 10 / 1284 data bit 3 / LCD data bit 11 / GPIO 35
AF5	gpio[36]	pull up	4	I/O	BD4CUIF	reserved / 1284 data bit 4 / LCD data bit 12 / GPIO 36
AD6	gpio[37]	pull up	4	I/O	BD4CUIF	reserved / 1284 data bit 5 / LCD data bit 13 / GPIO 37
AE5	gpio[38]	pull up	4	I/O	BD4CUIF	reserved / 1284 data bit 6 / LCD data bit 14 / GPIO 38
AF4	gpio[39]	pull up	4	I/O	BD4CUIF	reserved / 1284 data bit 7 / LCD data bit 15 / GPIO 39
AC6	gpio[40]	pull up	4	I/O	BD4CUIF	Ser port C TxData / Ext IRQ 3 / LCD data bit 16 / GPIO 40

AD5	gpio[41]	pull up	4	I/O	BD4CUIF	Ser port C RxData / Timer 11 / LCD data bit 17 / GPIO 41
AE4	gpio[42]	pull up	4	I/O	BD4CUIF	Ser port C RTS / Timer 12 / LCD data bit 18 / GPIO 42
AF3	gpio[43]	pull up	4	I/O	BD4CUIF	Ser port C CTS / Timer 13 / LCD data bit 19 / GPIO 43
AD2	gpio[44]	pull up	4	I/O	BD4CUIF	Ser port D TxData / 1284 periph on line / LCD data bit 20 / GPIO 44
AE1	gpio[45]	pull up	4	I/O	BD4CUIF	Ser port D RxData / 1284 data strobe / LCD data bit 21 / GPIO 45
AB3	gpio[46]	pull up	4	I/O	BD4CUIF	Ser port D RTS / 1284 auto line feed / LCD data bit 22 / GPIO 46
AA4	gpio[47]	pull up	4	I/O	BD4CUIF	Ser port D CTS / 1284 init / LCD data bit 23 / GPIO 47
AC2	gpio[48]	pull up	2	I/O	BD2CUIF	Timer 14 / 1284 periph select / DMA ch 1 req / GPIO 48
AD1	gpio[49]	pull up	2	I/O	BD2CUIF	Timer 15 / 1284 periph logic / DMA ch 1 done / GPIO 49

I2C Interface

Pin Number	Signal Name	OD (mA)	I/O	Buf Type	Description
AC15	iic_scl	4	I/O	BD4SCIF	I2C serial clock line
AF16	iic_sda	4	I/O	BD4SCIF	I2C serial data line

USB Interface

Pin Number	Signal Name	OD (mA)	I/O	Buf Type	Description
AB4	usb_dm		I/O	USB11C1	USB data -
AC3	usb_dp		I/O	USB11C1	USB data +

System Memory Interface

Pin Number	Signal Name	OD (mA)	I/O	Buf Type	Description
A21	addr[0]	8	O	BT8RIF	address bus signals
B20	addr[1]	8	O	BT8RIF	.
C19	addr[2]	8	O	BT8RIF	.
A20	addr[3]	8	O	BT8RIF	.
B19	addr[4]	8	O	BT8RIF	.
C18	addr[5]	8	O	BT8RIF	.
A19	addr[6]	8	O	BT8RIF	.
A17	addr[7]	8	O	BT8RIF	.
C16	addr[8]	8	O	BT8RIF	.
B16	addr[9]	8	O	BT8RIF	.
A16	addr[10]	8	O	BT8RIF	.
D15	addr[11]	8	O	BT8RIF	.
C15	addr[12]	8	O	BT8RIF	.
B15	addr[13]	8	O	BT8RIF	.
A15	addr[14]	8	O	BT8RIF	.
C14	addr[15]	8	O	BT8RIF	.
B14	addr[16]	8	O	BT8RIF	.
A14	addr[17]	8	O	BT8RIF	.
A13	addr[18]	8	O	BT8RIF	.
B13	addr[19]	8	O	BT8RIF	.
C13	addr[20]	8	O	BT8RIF	.
A12	addr[21]	8	O	BT8RIF	.
B12	addr[22]	8	O	BT8RIF	.
C12	addr[23]	8	O	BT8RIF	.
D12	addr[24]	8	O	BT8RIF	.
A11	addr[25]	8	O	BT8RIF	.
B11	addr[26]	8	O	BT8RIF	.
C11	addr[27]	8	O	BT8RIF	.
G2	clk_en[0]	8	O	BT8RIF	SDRAM clock enables
H3	clk_en[1]	8	O	BT8RIF	.
G1	clk_en[2]	8	O	BT8RIF	.
H2	clk_en[3]	8	O	BT8RIF	.
A10	clk_out[0]	8	O	BT8RIF	SDRAM clocks

A9	clk_out[1]	8	O	BT8RIF	.
A5	clk_out[2]	8	O	BT8RIF	.
A4	clk_out[3]	8	O	BT8RIF	.
G26	data[0]	8	I/O	BD8RCIF	data bus signals
H24	data[1]	8	I/O	BD8RCIF	.
G25	data[2]	8	I/O	BD8RCIF	.
F26	data[3]	8	I/O	BD8RCIF	.
G24	data[4]	8	I/O	BD8RCIF	.
F25	data[5]	8	I/O	BD8RCIF	.
E26	data[6]	8	I/O	BD8RCIF	.
F24	data[7]	8	I/O	BD8RCIF	.
E25	data[8]	8	I/O	BD8RCIF	.
D26	data[9]	8	I/O	BD8RCIF	.
F23	data[10]	8	I/O	BD8RCIF	.
E24	data[11]	8	I/O	BD8RCIF	.
D25	data[12]	8	I/O	BD8RCIF	.
C26	data[13]	8	I/O	BD8RCIF	.
E23	data[14]	8	I/O	BD8RCIF	.
D24	data[15]	8	I/O	BD8RCIF	.
C25	data[16]	8	I/O	BD8RCIF	.
B26	data[17]	8	I/O	BD8RCIF	.
D22	data[18]	8	I/O	BD8RCIF	.
C23	data[19]	8	I/O	BD8RCIF	.
B24	data[20]	8	I/O	BD8RCIF	.
A25	data[21]	8	I/O	BD8RCIF	.
C22	data[22]	8	I/O	BD8RCIF	.
D21	data[23]	8	I/O	BD8RCIF	.
B23	data[24]	8	I/O	BD8RCIF	.
A24	data[25]	8	I/O	BD8RCIF	.
A23	data[26]	8	I/O	BD8RCIF	.
B22	data[27]	8	I/O	BD8RCIF	.
C21	data[28]	8	I/O	BD8RCIF	.
A22	data[29]	8	I/O	BD8RCIF	.
B21	data[30]	8	I/O	BD8RCIF	.
C20	data[31]	8	I/O	BD8RCIF	.
E1	data_mask[0]	8	O	BT8RIF	SDRAM data mask signals
F2	data_mask[1]	8	O	BT8RIF	.
G3	data_mask[2]	8	O	BT8RIF	.
F1	data_mask[3]	8	O	BT8RIF	.
C5	clk_in[0]		I	IBUFIF	SDRAM feed-back clocks
D2	clk_in[1]		I	IBUFIF	.
E3	clk_in[2]		I	IBUFIF	.
E2	clk_in[3]		I	IBUFIF	.
B4	byte_lane_sel_n[0]	8	O	BT8RIF	Static memory byte lane select signals
F4	byte_lane_sel_n[1]	8	O	BT8RIF	.
D1	byte_lane_sel_n[2]	8	O	BT8RIF	.
F3	byte_lane_sel_n[3]	8	O	BT8RIF	.
B5	cas_n	8	O	BT8RIF	SDRAM column address strobe
A8	dy_cs_n[0]	8	O	BT8RIF	SDRAM chip select signals
B8	dy_cs_n[1]	8	O	BT8RIF	.
A6	dy_cs_n[2]	8	O	BT8RIF	.
C7	dy_cs_n[3]	8	O	BT8RIF	.

C6	st_oe_n		8	O	BT8RIF	Static memory output enable
D6	ras_n		8	O	BT8RIF	SDRAM row address strobe
H1	dy_pwr_n		8	O	BT8RIF	SyncFlash power down
B10	st_cs_n[0]		8	O	BT8RIF	Static memory chip select signals
C10	st_cs_n[1]		8	O	BT8RIF	.
B9	st_cs_n[2]		8	O	BT8RIF	.
C9	st_cs_n[3]		8	O	BT8RIF	.
B6	we_n		8	O	BT8RIF	SDRAM write enable
J3	ta_strb	pull up		I	IBUFUIF	Slow peripheral transfer acknowledge

Ethernet Interface

Pin Number	Signal Name		OD (mA)	I/O	Buf Type	Description
AB1	col			I	IBUFIF	Collision
AA2	crs			I	IBUFIF	Carrier sense
AC1	enet_phy_int_n	pull up		I	IBUFUIF	Ethernet phy interrupt
AA3	mdc		4	O	BT4IF	MII clock
AB2	mdio	pull up	2	I/O	BD2CUIF	MII data
T3	rx_clk			I	IBUFIF	Receive clock
V2	rx_dv			I	IBUFIF	Receive data valid
W1	rx_er			I	IBUFIF	Receive error
V1	rxd[0]			I	IBUFIF	Receive data bit 0
U3	rxd[1]			I	IBUFIF	Receive data bit 1
U2	rxd[2]			I	IBUFIF	Receive data bit 2
U1	rxd[3]			I	IBUFIF	Receive data bit 3
V3	tx_clk			I	IBUFIF	Transmit clock
AA1	tx_en		2	O	BT2IF	Transmit enable
Y3	tx_er		2	O	BT2IF	Transmit error
Y2	txd[0]		2	O	BT2IF	Transmit data bit 0
W3	txd[1]		2	O	BT2IF	Transmit data bit 1
Y1	txd[2]		2	O	BT2IF	Transmit data bit 2
W2	txd[3]		2	O	BT2IF	Transmit data bit 3

Clock Generation/System Pins

Pin Number	Signal Name		OD (mA)	I/O	Buf Type	Description
AF6	x1_vid_osc			I	OSCI	Video clock crystal oscillator circuit input
AE7	x2_vid_osc			O	OSCL40C10	Video clock crystal oscillator circuit output
C8	x1_sys_osc			I	OSCI	System clock crystal oscillator circuit input
B7	x2_sys_osc			O	OSCL40C10	System clock crystal oscillator circuit output
D9	x1_usb_osc			I	OSCI	USB clock crystal oscillator circuit input
A7	x2_usb_osc			O	OSCL60C10	USB clock crystal oscillator circuit output
AC21	reset_done	pull up	2	I/O	BD2CUIF	System reset done signal, CPU enabled when asserted
H25	reset_n	pull up		I	IBUFUIF	System reset input signal
AD20	bist_en_n			I	IBUFIF	Enable internal bist operation
AF21	pll_test_n			I	IBUFIF	Enable PLL testing
AE21	scan_en_n			I	IBUFIF	Enable internal scan testing
AD4	vid_pll_dvdd				ZSAPLVDCR	Video clock PLL 1.5V digital power
AC5	vid_pll_dvss				ZSAPLVSCR	Video clock PLL digital ground
AF2	vid_pll_avdd				ZSAPLVDRR	Video clock PLL 3.3V analog power
AE3	vid_pll_avss				ZSAPLVSLR	Video clock PLL analog ground
B18	sys_pll_dvdd				ZSAPLVDCR	System clock PLL 1.5V digital power
A18	sys_pll_dvss				ZSAPLVSCR	System clock PLL digital ground
B17	sys_pll_avdd				ZSAPLVDRR	System clock PLL 3.3V analog power
C17	sys_pll_avss				ZSAPLVSLR	System clock PLL analog ground
J2	lcdclk	pull up		I	IBUFUIF	External LCD clock input

JTAG Interface for ARM Core / Boundary Scan						
Pin Number	**Signal Name**		**OD (mA)**	**I/O**	**Buf Type**	**Description**
AE20	tck			I	IBUFIF	Test clock
AD18	tdi	pull up		I	IBUFUIF	Test data in
AE19	tdo		2	O	BT2IF	Test data out
AC18	tms	pull up		I	IBUFUIF	Test mode select
AF20	trst_n	pull up		I	IBUFUIF	Test mode reset
AD19	rtck	pull up	2	I/O	BD2CUIF	Returned test clock, ARM core only

Unconnects	
Pin Number	
AF22	no connect
AD21	no connect
AE22	no connect

Power/Ground		
Pin Number	**Signal Name**	**Description**
J23	VDDC	Core power, 1.5V
L23	VDDC	.
K23	VDDC	.
U23	VDDC	.
T23	VDDC	.
V23	VDDC	.
D18	VDDC	.
D17	VDDC	.
AC17	VDDC	.
D16	VDDC	.
AC16	VDDC	.
D11	VDDC	.
D10	VDDC	.
AC11	VDDC	.
AC10	VDDC	.
AC9	VDDC	.
J4	VDDC	.
L4	VDDC	.
K4	VDDC	.
U4	VDDC	.
T4	VDDC	.
V4	VDDC	.
G23	VDDS	I/O power, 3.3V
H23	VDDS	.
M23	VDDS	.
R23	VDDS	.
P23	VDDS	.
N23	VDDS	.
Y23	VDDS	.
W23	VDDS	.
D20	VDDS	.
AC20	VDDS	.
D19	VDDS	.
AC19	VDDS	.
D14	VDDS	.
D13	VDDS	.
AC14	VDDS	.

AC13	VDDS	.
D8	VDDS	.
D7	VDDS	.
AC8	VDDS	.
AC7	VDDS	.
G4	VDDS	.
H4	VDDS	.
M4	VDDS	.
R4	VDDS	.
P4	VDDS	.
N4	VDDS	.
Y4	VDDS	.
W4	VDDS	.
A26	VSS2	Ground
B25	VSS2	.
AE25	VSS2	.
AF26	VSS2	.
D23	VSS2	.
C24	VSS2	.
AD24	VSS2	.
AC23	VSS2	.
D5	VSS2	.
D4	VSS2	.
C4	VSS2	.
E4	VSS2	.
AC4	VSS2	.
A3	VSS2	.
A2	VSS2	.
D3	VSS2	.
C3	VSS2	.
C2	VSS2	.
B3	VSS2	.
B2	VSS2	.
AE2	VSS2	.
AD3	VSS2	.
A1	VSS2	.
C1	VSS2	.
B1	VSS2	.
AF1	VSS2	.

Print Engine Interface

Pin Number	Signal Name	Pull Up/Down	OD (mA)	I/O	Buf Type	Description
N3	bp_stat_0	pull up	2	I/O	BD2CUIF	channel 0 bypass status bit 1
P1	bp_stat_1	pull up	2	I/O	BD2CUIF	channel 1 bypass status bit 1
P2	bp_stat_2	pull up	2	I/O	BD2CUIF	channel 2 bypass status bit 1
P3	bp_stat_3	pull up	2	I/O	BD2CUIF	channel 3 bypass status bit 1
J1	hsync_0			I	IBUFIF	channel 0 horizontal sync
K3	hsync_1			I	IBUFIF	channel 1 horizontal sync
K2	hsync_2			I	IBUFIF	channel 2 horizontal sync
K1	hsync_3			I	IBUFIF	channel 3 horizontal sync
M2	vsync_0		2	I/O	BD2CIF	channel 0 vertical sync / channel 0 bypass status bit 0
M1	vsync_1		2	I/O	BD2CIF	channel 1 vertical sync / channel 1 bypass status bit 0
N1	vsync_2		2	I/O	BD2CIF	channel 2 vertical sync / channel 2 bypass status bit 0

N2	vsync_3		2	I/O	BD2CIF	channel 3 vertical sync / channel 3 bypass status bit 0
R1	vclk_0			I	IBUFIF	channel 0 video clock
R2	vclk_1			I	IBUFIF	channel 1 video clock
R3	vclk_2			I	IBUFIF	channel 2 video clock
T1	vclk_3			I	IBUFIF	channel 3 video clock
L3	video_data_0		8	O	BT8IF	channel 0 serial video data
L2	video_data_1		8	O	BT8IF	channel 1 serial video data
L1	video_data_2		8	O	BT8IF	channel 2 serial video data
M3	video_data_3		8	O	BT8IF	channel 3 serial video data
T2	print	pull up	2	I/O	BD2CUIF	print control output