CPU Speed = 100.00Mhz, Memory Bus Speed = 50.00Mhz (Period = 20.00ns)

Reference Oscillator = 50.00Mhz, PLL Multiplier = 16 (ND = 15), PLL Output Divider = 4 (FS = 2)

Component	Register Name	Register Mnemonic	Register Address	Register Value	Comments
Global SDRAM Settings					PC133 SDRAM ; CAS=2 ; -7E (Chip) or -13E (DIMM)
	Control	MPMCControl	0xA070_0000	0x0000_0001	
	Status	MPMCStatus	0xA070_0004	Read-Only	
	Configuration	MPMCConfig	0xA070_0008	User Defined	Field CLK must be set to 0
	Dynamic Memory Control	MPMCDynamicControl	0xA070_0020	0x0000_0000	See SDRAM initialization in HRM
	Dynamic Memory Refresh Timer	MPMCDynamicRefresh	0xA070_0024	0x0000_000C	
	Dynamic Memory Read Configuration	MPMCDynamicReadConfig	0xA070_0028	0x0000_0001	
	Dynamic Memory Precharge Command Period	MPMCDynamictRP	0xA070_0030	0x0000_0000	
	Dynamic Memory Active To Precharge Command Period	MPMCDynamictRAS	0xA070_0034	0x0000_0001	
	Dynamic Memory Self-refresh Exit Time	MPMCDynamictSREX	0xA070_0038	0x0000_0003	
	Dynamic Memory Last Data Out To Active Time	MPMCDynamictAPR	0xA070_003C	0x0000_0000	MPMCDynamictRP - 1
	Dynamic Memory Data-in To Active Command Time	MPMCDynamictDAL	0xA070_0040	0x0000_0004	MPMCDynamictWR + MPMCDynamictRP + 2
	Dynamic Memory Write Recovery Time	MPMCDynamictWR	0xA070_0044	0x0000_0001	
	Dynamic Memory Active To Active Command Period	MPMCDynamictRC	0xA070_0048	0x0000_0002	
	Dynamic Memory Auto-refresh Period	MPMCDynamictRFC	0xA070_004C	0x0000_0003	
	Dynamic Memory Exit Self-refresh	MPMCDynamictXSR	0xA070_0050	0x0000_0003	
	Dynamic Memory Active Bank A to Active Bank B Time	MPMCDynamictRRD	0xA070_0054	0x0000_0000	
	Dynamic Memory Load Mode Register To Active Command Time	MPMCDynamictMRD	0xA070_0058	0x0000_0002	

Component	Register Name	Register Mnemonic	Register Address	Register Value	Comments
MT48LC16M16A2					Micron 256Mb PC133 SDRAM ; 16Mx16 ; 2 Chips
	Dynamic Memory Configuration Register #0	MPMCDynamicConfig0	0xA070_0100	0x0008_4680	See SDRAM initialization in HRM
	Dynamic Memory RAS and CAS Delay Register #0	MPMCDynamicRasCas0	0xA070_0104	0x0000_0202	For SDRAM init AHB ADDR = 0x0004_4000

Component	Register Name	Register Mnemonic	Register Address	Register Value	Comments
MT48LC32M16A2					Micron 512Mb PC133 SDRAM ; 32Mx16 ; 2 Chips
	Dynamic Memory Configuration Register #1	MPMCDynamicConfig1	0xA070_0120	0x0008_4880	See SDRAM initialization in HRM
	Dynamic Memory RAS and CAS Delay Register #1	MPMCDynamicRasCas1	0xA070_0124	0x0000_0202	For SDRAM init AHB ADDR = 0x1008_8000

Component	Register Name	Register Mnemonic	Register Address	Register Value	Comments
MT8LSDT3264A					Micron 256MB PC133 DIMM ; 32Mx64 ; 2 chip selects required
	Dynamic Memory Configuration Register #2	MPMCDynamicConfig2	0xA070_0140	0x0008_4600	See SDRAM initialization in HRM
	Dynamic Memory RAS and CAS Delay Register #2	MPMCDynamicRasCas2	0xA070_0144	0x0000_0202	For SDRAM init AHB ADDR = 0x2008_8000
	Dynamic Memory Configuration Register #3	MPMCDynamicConfig3	0xA070_0160	0x0008_4600	See SDRAM initialization in HRM
	Dynamic Memory RAS and CAS Delay Register #3	MPMCDynamicRasCas3	0xA070_0164	0x0000_0202	For SDRAM init AHB ADDR = 0x3008_8000

Component	Register Name	Register Mnemonic	Register Address	Register Value	Comments
Global SRAM Settings					All asyncronous access memories are considered SRAM
	Static Memory Extended Wait	MPMCStaticExtendedWait	0xA070_0080	User Defined	Only necessary for slow asccess SRAM-like external peripherals

Component	Register Name	Register Mnemonic	Register Address	Register Value	Comments
M29W320DT					ST-Micro 32Mb Flash ; 2Mbx16 ; 2 Chips ; 70ns access time
	Static Memory Configuration Register #1	MPMCStaticConfig1	0xA070_0220	0x0000_0002	
	Static Memory Write Enable Delay Registers #1	MPMCStaticWaitWen1	0xA070_0224	0x0000_0000	
	Static Memory Output Enable Delay Registers #1	MPMCStaticWaitOen1	0xA070_0228	0x0000_0000	
	Static Memory Read Delay Registers #1	MPMCStaticWaitRd1	0xA070_022C	0x0000_0004	70ns access time + 20ns for propagation and setup delays
	Static Memory Page Mode Read Delay Registers #1	MPMCStaticWaitPage1	0xA070_0230	0x0000_0000	This part does not support page mode access
	Static Memory Write Delay Registers #1	MPMCStaticWaitWr1	0xA070_0234	0x0000_0002	
	Static Memory Turn Round Delay Registers #1	MPMCStaticWaitTurn1	0xA070_0238	0x0000_0000	