NS7520 BCLK Speed Errata -1/2 or 64MHz (Or higher) Application Note

Change History
Version Date Summary
Rev 0.1 02/09/05 DRAFT copy for Internal Review
Rev 0.2 10/17/05 Page 3 - Changed "40ns (0.8V to 2.0V) " to "18ns (0.8V to 2.0V) "

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1. Introduction

When the NS7520 is configured to use the PLL clock generator, the system clock can come up at ½ the configured frequency, or at a higher frequency - Usually 64MHz.

When the PLLTST and BISTEN signals are set high with the SCANEN signal low, the PLL clock generator should produce the system clock based on the code it reads on address signals A[4:0]. On rare occasions the system clock will be ½ the frequency, or greater than the configured frequency due to the internal PLL circuitry not being properly reset.

When the PLL is bypassed; PLLTST_N, BISTEN_N, SCANEN_N all equal to a logic "1", this application note not does not apply.

2. Work Around

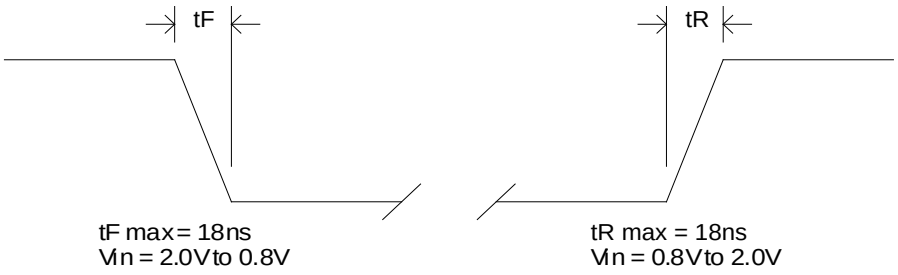
Insuring that the RESET source has adequate fall/rise times and is free from glitches & ringing is a requirement to prevent the 64MHz or other higher frequency. See Figure 1.

Inverting the active LVTTL RESET_N signal and attaching it to the SCANEN_N pin prevents the ½ BCLK failure. The maximum delay (inverter propagation delay plus the etch delay) between pins A10 and L13 must be less than 8ns. See Figure 2.

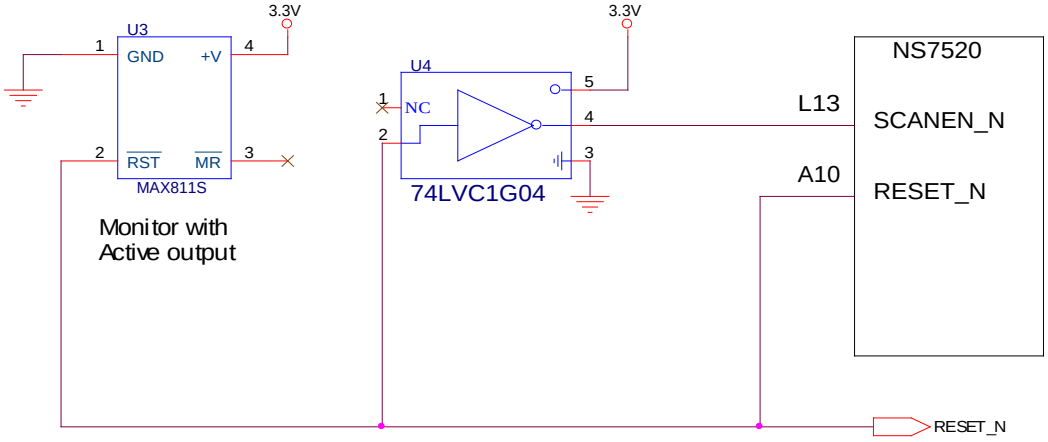
Most open drain power monitors require a speedup circuit in order to met the fall/rise timing. See Figure 3.

An external RESET_N source with a Rise time exceeding 40ns (0.8V to 2.0V) should use a Schmitt trigger speedup circuit such as a 74LVC2G14.

3. Figure 1: Rise/fall timing



4. Figure 2: SCANNEN inverter with Active TTL monitor



5. Figure 3: RESET speed up with Open Drain monitor