NS9750B-A1

Thank you for purchasing the NS9750 development kit. Note that your development board is built using the first version of the NS9750 processor, with a part marking of NS9750B-0-C200. The first version had a problem that required use of an external clock to drive the PLL, as well as five other errata. NetSilicon has created an improved version of the processor which resolves the PLL issue and the five errata. The differences are outlined in this document.

We encourage you to continue your development and to review the processor changes, and to finalize your design by using the new processor. The new processor is differentiated with a marking of NS9750B-A1 (with appropriate temperature and speed markings). Five free samples are included with your development kit.

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NS9750B-A1

- What's different?
- Errata fixes
- Impact on NS9750B-0
- Order codes

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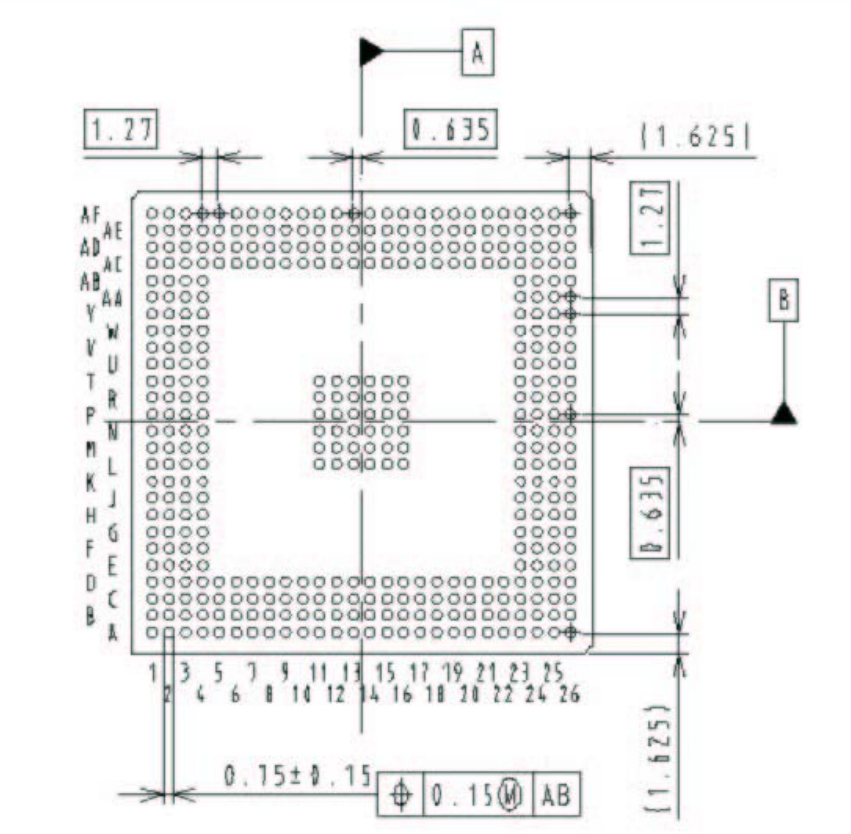
NS9750B-A1
36 new pins



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NS9750B-A1
17 pin changes

From 1.5v to Ground		From 3.3v to Ground	
L23	T23	M23	R23
D18	AC9	D19	AC19
L4	T4	D8	AC8
		M4	R4

Feedback clock to sreset_n

D2 - was clk_in[1], now sreset_n

E3 - was clk_in[2], now sreset_n_enable

E2 - was clk_in[3], now tie to GND

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NS9750B-A1

- PLL is stable
- Four errata are confirmed fixed
- PLL bypass mode cannot be used
- BOM cost reduction

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Errata: Fixed

- RTS assertion
- JTAG assert reset
- Gap timers in PLL bypass mode*
- USB PHY: low speed
- Modem signal inversion

* Bypass mode cannot be used

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Migrate from NS9750B-0?

- BOM cost reduction ~$4-5 (no external PLL components)
- Primary customers will transition
- No plan to obsolete NS9750B-0

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Order Codes

- To order additional product:
  - NS9750B-A1-C200
  - NS9750B-A1-C125
  - NS9750B-A1-I162

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Errata Details

1. RTS not asserted during transmit on serial channels A and D

The control signal that asserts "RTS-only" while transmitting is miswired for serial channels A and D, but is wired correctly for channels B and C. This means that RTS is not asserted properly while transmitting when the RTSTX control bit is set in Control Register B.

2. Debugger asserting reset_n causes system lockup

System reset input signal reset_n inhibits JTAG operation while active, causing lockup with debugger. The lockup occurs because the debugger expects JTAG to be operational while reset_n is active, according to the IEEE1149.1 specification.

Workaround: The debugger must pulse reset_n once. On the 20-pin JTAG connector, this is nSRST on pin 15. A power cycle or the board's RESET button should be used to reset the NS9750. Basic debug features are still available.

When using the EPI Majic debugger in the Target Interface Properties window, do not check *Reset target using Reset Output Signal.*

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Errata Details

3. Serial port buffer GAP timer non-functional in PLL bypass mode

Serial port buffer GAP timers do not function in PLL bypass mode. (These timers are used to close a receive buffer when a few bytes remain in the FIFO and the line is quiet for a specified period.)

4. USB PHY cannot be placed into low speed in device mode

The FSEN input to the USB PHY is fixed at 0 (high speed mode) when the NS9750 is configured**.**

5. Modem control signals are inverted

These serial signals in the NS9750 are inverted from conventional serial logic: RTS, CTS, DSR, DTR, DI, and DCD. As a standard, a 1 in the control or status register is an active state for the signal. Serial signals are active in the *space* condition, which is a logic low, or a positive voltage on a 232 line after passing through the line driver. The NS9750 has this standard reversed, so a 1 in a register matches with a logic high and a mark (negative voltage) condition on the 232 line.

Workaround: When used, the affected signals must be inverted externally. These inverters will be added to final NS9750 development boards.

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