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1. History

Date	Version	Responsible	Description
18/02/05	1.0	K Rudolf	Initial Version
07.03.2005	1.1	K Rudolf	Ethernet LEDs need external resistor
09.03.2005	1.2	K Rudolf	Restructuring showing state after U-Boot
19.05.2005	2.0	K Rudolf	A9M9360_2: Pull up 10K to +3.3V at RSTIN# added

2. Preface

A9M9360 Module is a member of the ARM9 family with CPUs of different manufactorers. It has a NetSilicon NS9360 CPU, a 32-bit machine with up to 177MHz clock speed. The tables in the next sides describe every pin of the 2 X 120 pole connectors of the module, its properties and the usage of it on the A9M9750DEV_1 board.

3. Module A9M9360 Pinning

Legend pin specification in table:

X1	Type	U-Boot	RESET State	A9M9360 Name	A9M9360 Description after UBOOT	Application A9M9750DEV_1
				module specific pins		
				common pins to all A9M modules		

Legend Type:
I: Input
O: Output
I/O: Input or Output
P: Power

Legend RESET State:
PUW: Weak pull up to switched 3.3V in CPU on module
PU10: Pull up 10K to switched 3.3V on module

Legend A9M9360 Name:
GPIO names show GPIO/Function0_UART/Function0_misc/Function1/Function2
GPIOSWX: no connection to GPIOX, when RESET# asserted (is strapping pin)

3.1. Connector X1

X1	Type	U-Boot	RESET State	A9M9360 Name	A9M9360 Description after UBOOT	Application A9M9750DEV_1
1	P	-	-	GND		
2	I	-	PU10	RSTIN#	Reset Input, i.e. Push Button on the module this signal is the input to a reset controller Pullup 10K to +3.3V on module	Connected via 470R output RES# RESET controller U16 supervising 1.5V, 3.3V and manual RESET push button on DEV board
3	I/O	-		PWRGOOD	Output of the reset controller push pull with 470R current limiting resistor	Connected as PWRGOOD to Multi-ICE X13 pin 15
4	O	RSTOUT#		RSTOUT#	Output of CPU RESET_DONE logical ANDed with PWRGOOD: High after SPI boot loading finished	Connected as RSTOUT# to FPGA and CPLD
5	I	-	PU10	TCK	JTAG	Connected to X12 (JTAG Booster), X13 (Multi-ICE)
6	I	-	PU10	TMS	JTAG	Connected to X12 (JTAG Booster), X13 (Multi-ICE)
7	I	-	PU10	TDI	JTAG	Connected to X12 (JTAG Booster), X13 (Multi-ICE)
8	O	-	PU10	TDO	JTAG	Connected to X12 (JTAG Booster), X13 (Multi-ICE)
9	I	-	PU10	TRST#	JTAG	Connected to X12 (JTAG Booster), X13 (Multi-ICE)
10	I	-	PU10	CONF0/ DEBUGEN#	Debug Enable, 0 = Debug enabled, TRST# isolated from SRST#	Connected to DIP-switch S4.1 ON: connected to GND
11	I	-	PU10	CONF1/ NAND_FWP#	NAND Flash Write Protect, 0 = NAND Flash write protected	Connected to DIP-switch S4.2 ON: connected to GND
12	I	-	PU10	CONF2/ OCD_EN#	Enables OCD mode, use with CONF0; Pullup 10k to +3.3V on module	Connected to DIP-switch S4.3 ON: connected to GND
13	-	-	-	CONF3/ not used	no function n.c.	Connected to DIP-switch S4.4 ON: connected to GND
14	I/O	I	PU10	CONF4 GPIO38; 2K2 in serie Bit28 GEN_ID		Connected to DIP-switch S4.5 ON: connected to GND
15	I/O	I	PU10	CONF5 GPIO39; 2K2 in serie Bit29 GEN_ID		Connected to DIP-switch S4.6 ON: connected to GND
16	I/O	I	PU10	CONF6 GPIO40; 2K2 in serie Bit30 GEN_ID		Connected to DIP-switch S4.7 ON: connected to GND
17	I/O	I	PU10	CONF7 GPIO41; 2K2 in serie Bit31 GEN_ID		Connected to DIP-switch S4.8 ON: connected to GND
18	I/O		PU10	GPIOSW8/ TXDA/ SPIA_DO/ -/ -	GPIO Input	Connected as SPIA_DO (Funct 0, SPI) to Touch Controller LCD, X27
19	I/O		PUW	GPIO9/ RXDA/ SPIA_DI -/ -	GPIO Input	Connected as SPIA_DI (Funct 0, SPI) to Touch Controller LCD, X27
20	I/O		PU10	GPIOSW10/ RTSA#/ -/ reserved/ PWM0 dupe	GPIO Input	Connected as AUD_WS (FUNCT 3, Output) to Audio chip U6
21	I/O		PUW	GPIO11/ CTSA#/ -/ EIRQ2 dupe/ timer 0 dupe	GPIO Input	Connected as IRQ2 (Input, Funct 1) to FPGA U17 and CPLD U2, pull up 10K on DEV

X1	Type	U-Boot	RESET State	A9M9360 Name	A9M9360 Description after UBOOT	Application A9M9750DEV_1
22	I/O	-	PU10	GPIOSW12/ DTRA#/ -/ reserved/ PWM1 dupe	GPIO Input	Connected as FPGA_CS0# (Output, Funct 3) via switch U41 to FPGA EEPROM U10
23	I/O	-	PU10	GPIO13/ DSRA#/ -/ EIRQ0 dupe/ PWM2 dupe	GPIO Input	Connected to RTC_INT# on Module; logical OR with open drain possible
24	I/O	TxDB	PU10	GPIOSW0/ TXDB/ SPIB_DO DMA0_DONE dupe/ timer 1 dupe	TXD Console (Output, Funct 0, UART)	Connected as SPIB_DO (Output Funct 0, SPI) to audio chip U6
25	I/O	RxDB	PUW	GPIO1/ RXDB/ SPIB_DI/ DMA0_REQ dupe EIRQ0	RXD Console (Input, Funct 0, UART)	Connected as SPIB_DI (Input Funct 0, SPI) via R58 to audio chip U6
26	I/O		PU10	GPIOSW2/ RTSB#/ -/ timer0/ DMA1_ACK	GPIO Input	Connected as L3_CLK (Output, Funct 3) to audio chip U6
27	I/O		PUW	GPIO3/ CTSB#/ -/ 1284_ACK#/ DMA0_REQ#	GPIO Input	Connected as DMA_REQ0 (Input, Funct 2) to FPGA U17 and CPLD U2
28	I/O	-	PU10	GPIOSW4/ DTRB#/ -/ 1284_BUSY/ DMA0_DONE	GPIO Input	Connected as L3MODE (Output, Funct 3) to audio chip U6
29	I/O	-	PUW	GPIO5/ DSRB#/ -/ 1284_ERR DMA0_ACK	GPIO Input	Connected as DMA_ACK0 (Output, Funct 2) to FPGA U17 and CPLD U2
30	I/O	-	PUW	GPIO6/ RIB#/ SPIB_CLK/ 1284P_JAM/ timer 7 dupe	GPIO Input	Connected as SPIB_CLK (Funct 0, SPI) to audio chip U6 and FPGA U17
31	I/O	-	PUW	GPIO7/ DCDB#/ SPIB_EN/ DMA0_ACK dupe/ EIRQ1	GPIO Input	Connected as SPIB_EN# (Funct0, SPI) to FPGA U17
32	I/O	-	-	GPIO72/ -/ WAIT#/ reserved/ reserved	GPIO Input	Connected as WAIT# (Input, Funct 0) to FPGA U17 and CPLD U2
33	I/O	-	-	GPIO68/ -/ A24/ MCKE_0/ EIRQ0 dupe	GPIO Input	Connected as A24 (Output, Funct 0) to FPGA U17
34	I/O	-	-	GPIO69/ -/ A25/ MCKE_1/ EIRQ1 dupe	GPIO Input	Connected as A25 (Output, Funct 0) to FPGA U17
35	-	-	-	n.c.	reserved for A26	
36	-	-	-	n.c.	reserved for A27	
37	I/O	I/O	PUW	GPIOSW24/ DTRD#/ -/ LCDD0/ reserved	LCD data	Connected as LCDD0 (I/O, Funct 1) to X25

X1	Type	U-Boot	RESET State	A9M9360 Name	A9M9360 Description after UBOOT	Application A9M9750DEV_1
38	I/O	I/O	PUW	GPIO25/ DSRD#/ -/ LCDD1/ reserved	LCD data	Connected as LCDD1 (I/O, Funct 1) to X25
39	P	P	-	GND		
40	I/O	I/O	PUW	GPIO26/ RID#/ SPID_CK/ LCDD2/ timer 3	LCD data	Connected as LCDD2 (I/O, Funct 1) to X25
41	I/O	I/O	PUW	GPIO27/ DCDD#/ SPID_EN#/ LCDD3/ timer 4	LCD data	Connected as LCDD3 (I/O, Funct 1) to X25
42	I/O	I/O	PUW	GPIO28/ -/ EIRQ1 dupe/ LCDD4/ LCDD8 dupe	LCD data	Connected as LCDD4 (I/O, Funct 1) to X25
43	I/O	I/O	PUW	GPIO29/ -/ timer 5/ LCDD5/ LCDD9 dupe	LCD data	Connected as LCDD5 (I/O, Funct 1) to X25
44	I/O	I/O	PUW	GPIO30/ -/ timer 6 LCDD6/ LCDD10 dupe	LCD data	Connected as LCDD6 (I/O, Funct 1) to X25
45	I/O	I/O	PUW	GPIO31/ -/ timer 7/ LCDD7/ LCDD11 dupe	LCD data	Connected as LCDD7 (I/O, Funct 1) to X25
46	I/O	I/O	PUW	GPIO32/ -/ EIRQ2/ 1284_D0/ LCDD8	LCD data	Connected as LCDD8 (I/O, Funct 1) to X25
47	I/O	I/O	PUW	GPIO33/ -/ reserved/ 1284_D1/ LCDD9	LCD data	Connected as LCDD9 (I/O, Funct 1) to X25
48	I/O	I/O	PUW	GPIO34/ -/ I2C_SCL/ 1284_D2/ LCDD10	LCD data	Connected as LCDD10 (I/O, Funct 1) to X25
49	I/O	I/O	PUW	GPIO35/ -/ I2C_SDA/ 1284_D3/ LCDD11	LCD data	Connected as LCDD11 (I/O, Funct 1) to X25
50	I/O	I/O	PU10	GPIOSW36/ -/ PWM0/ 1284_D4/ LCDD12	LCD data	Connected as LCDD12 (I/O, Funct 1) to X25
51	I/O	I/O	PU10	GPIOSW37/ -/ PWM1/ 1284_D5/ LCDD13	LCD data	Connected as LCDD13 (I/O, Funct 1) to X25
52	I/O	I/O	PU10	GPIOSW38/ -/ PWM2/ 1284_D6/ LCDD14	LCD data	Connected as LCDD14 (I/O, Funct 1) to X25

X1	Type	U-Boot	RESET State	A9M9360 Name	A9M9360 Description after UBOOT	Application A9M9750DEV_1
53	I/O	I/O	PU10	GPIOSW39/ -/ PWM3/ 1284_D7/ LCDD15	LCD data	Connected as LCDD15 (I/O, Funct 1) to X25
54	I/O	I/O	PU10	GPIOSW40/ TXDC/ SPIC_DO/ EIRQ3/ LCDD16	LCD data	Connected as LCDD16 (I/O, Funct 1) to X25
55	I/O	I/O	PU10	GPIOSW41/ RXDC/ SPIC_DI/ reserved/ LCDD17	LCD data	Connected as LCDD17 (I/O, Funct 1) to X25
56	I/O	-	PUW	GPIO42/ RTSC#/ -/ reserved/ USB_EXTPHY_D+	GPIOInput	Connected as FPGA_DCLK (Output, Funct 3) via switch U41 to FPGA EEPROM U10 or as USB_PHY_DP (I/O, Funct 2) to USB PHY U20
57	I/O	-	PUW	GPIO43/ CTSC#/ -/ 1284_DIRCON/ USB_EXTPHY_D-	GPIO Input	Connected as FPGA_DATA0 (Input, Funct 3) via switch U40 to FPGA EEPROM U10 or as USB_PHY_DM (I/O, Funct 2) to USB PHY U20
58	I/O	-	PU10	GPIOSW44/ TXDD/ SPID_DO/ 1284_SELECT/ USB_EXTPHY_OE#	GPIO Input	Connected as FPGA_ASD0 (Output, Funct 3) via switch U41 to FPGA EEPROM U10 or as USB_PHY_OE# (Output, Funct 2) to USB PHY U20
59	I/O	-	PUW	GPIO45/ RXDD/ SPID_DI/ 1284_STB/ USB_EXTPHY_RCV	GPIO Input	Connected as GPIO45 (Input, Funct 3) via 1K (R89) to U1 (user key 1) and as USB_PHY_RCV (Input, Funct 2) to USB PHY U20
60	I/O	-	PUW	GPIO46/ RTSD#/ -/ 1284_ALFD USB_EXTPHY_RXD+	GPIO Input	Connected as GPIO46 (Input, Funct 3) via 1K (R90) to U2 (user key 2)
61	O	GPIO47	PUW	GPIO47/ CTSD#/ -/ 1284_INIT/ USB_EXTPHY_RXD-	GPIO Output	Connected as GPIO47 (Output, Funct 3) via J13 to LE4 (DEBUG LED)
62	I/O	I	PUW	GPIO18/ -/ ECAM_REJ/ LCD_PWREN#/ EIRQ3 dupe	LCD Control Output	Connected as LCD_PWREN# (Output, Funct 1 or Funct 3) to X25
63	I/O	I	PUW	GPIO22/ RIC#/ SPIC_CK/ LCD_AC_BDE/ reserved	LCD Output	Connected as LCD_AC_BDE (Output, Funct 1) to X25
64	I/O	I	PUW	GPIO21/ DSRC#/ -/ LCD_FRAME/ reserved	LCD Output	Connected as LCD_FRAME (Outputm Funct 1) to X25
65	I/O	I	PU10	GPIOSW19/ -/ ECAM_REQ/ LCD_HSYNC/ DMA1_ACK	LCD Output	Connected as LCD_HSYNC (Output, Funct 1) to X25
66	I/O	I	PU10	GPIOSW20/ DTRC#/ -/ LCD_CLK/ reserved	LCD Output	Connected as LCD_CLK (Output, Funct 1) to X25

X1	Type	U-Boot	RESET State	A9M9360 Name	A9M9360 Description after UBOOT	Application A9M9750DEV_1
67	I/O	I	PUW	GPIO23/ DCDC#/ SPIC_EN#/ LCD_LEND/ reserved	LCD Output	Connected as LCD_LEND (Output, Funct 1) to X25
68	O	-		A0	external address	Connected to FPGA U17 and CPLD U2
69	O	-		A1	external address	Connected to FPGA U17 and CPLD U2
70	O	-		A2	external address	Connected to FPGA U17 and CPLD U2
71	O	-		A3	external address	Connected to FPGA U17 and CPLD U2
72	O	-		A4	external address	Connected to FPGA U17 and CPLD U2
73	O	-		A5	external address	Connected to FPGA U17 and CPLD U2
74	O	-		A6	external address	Connected to FPGA U17 and CPLD U2
75	O	-		A7	external address	Connected to FPGA U17 and CPLD U2
76	O	-		A8	external address	Connected to FPGA U17
77	O	-		A9	external address	Connected to FPGA U17
78	O	-		A10	external address	Connected to FPGA U17
79	P	-	-	GND		
80	O	-		A11	external address	Connected to FPGA U17
81	O	-		A12	external address	Connected to FPGA U17
82	O	-		A13	external address	Connected to FPGA U17
83	O	-		A14	external address	Connected to FPGA U17
84	O	-		A15	external address	Connected to FPGA U17
85	O	-		A16	external address	Connected to FPGA U17
86	O	-		A17	external address	Connected to FPGA U17
87	O	-		A18	external address	Connected to FPGA U17
88	O	-		A19	external address	Connected to FPGA U17
89	O	-		A20	external address	Connected to FPGA U17
90	O	-		A21	external address	Connected to FPGA U17
91	O	-		GPIO66/ -/ A22/ reserved/ reserved	Set to external address	Connected as A22 (Output, Funct 0) to FPGA U17
92	O	-		EXT_OE#	Bus control	Connected to FPGA U17and CPLD U2
93	O	-		EXT_WE#	Bus control, 22R series resistor on module	Connected to FPGA U17 and CPLD U2
94	O	-		GPIO67/ -/ A23/ reserved/ reserved	Set to external address	Connected as A23 (Output, Funct 0) to FPGA U17
95	O	CS0#		CS0#	Chip select, not used on module, Defaults to Ouput/High at reset.	Connected to FPGA U17 and CPLD U2
96	O	CS2#		CS2#	Chip select, not used on module, Defaults to Ouput/High at reset.	Connected to FPGA U17 and CPLD U2
97	O	CS3#		CS3#	Chip select, not used on module, Defaults to Ouput/High at reset.	Connected to FPGA U17 and CPLD U2
98	-	-	-	NC	-	
99	O	-	-	PWREN	power sequencing control, high if 3.3V enabled	switches +3.3V on board
100	-	-	-	NC (reserved as BATT_FLT#)	-	
101	I/O	-	PUW	GPIO48/ -/ USB_EXTPHY_SUSP/ 1284P_SEL/ DMA1_REQ	GPIO Input	Connected as USB_EXTPHY_SUSP (Output, Funct 0) to USB PHY U20

X1	Type	U-Boot	RESET State	A9M9360 Name	A9M9360 Description after UBOOT	Application A9M9750DEV_1
102	I	-	PUW	GPIO16/ -/ USB_OVC/ 1284P_JAM dupe/ reserved	GPIO Input	Connected as USB_OVRCURR (Input, Funct 3) to U8
103	O	-	No	EXT_BE0#	Upper Byte/Lower Byte Enable	Connected as EXT_BE0# to FPGA U17
104	O	-	No	EXT_BE1#	Upper Byte/Lower Byte Enable	Connected as EXT_BE1# to FPGA U17
105	O	-	No	EXT_BE2#	Upper Byte/Lower Byte Enable	Connected as EXT_BE2# to FPGA U17
106	O	-	No	EXT_BE3#	Upper Byte/Lower Byte Enable	Connected as EXT_BE3# to FPGA U17
107	I	-	PUW	GPIO15/ DCDA#/ SPIA_EN#/ timer 2/ LCD_CLKIN	GPIO Input	Connected as SPIA_EN# (Input, Funct 0 SPI) to X27 (touch)
108	-	-	-	NC	-	
109	-	-	-	NC	-	
110	I	SPICLK0	No	GPIO14/ RIA#/ SPIA_CLK/ timer 1/ PWM3 dupe	GPIO Input	Connected as SPIA_CLK (Input, Funct 0 SPI) to X27 (touch)
111	O	I2C_SCL	-	GPIO70/ -/ A26/ MCKE_2/ I2C_SCL	used as I2C_SCL (Funct 2) on A9M9360, pull up 4K7 to switched 3.3V on module	accessible on X11, C28
112	I/O	I2C_SDA	-	GPIO71/ -/ A27/ MCKE_3/ I2C_SDA	used as I2C_SDA (Funct 2) on A9M9360, pull up 4K7 to switched 3.3V on module	accessible on X11, D28
113	I/O	I	PU10	GPIOSW17/ -/ USB_PWR	GPIO Input	USB device: GPIO17 output to switch on 1k5 pull-up resistor
114	I/O	USBP	No	USB_INTPHY_P	USB host or device from internal PHY	USB data line +, connected via R95 to expansion connector X10
115	I/O	USBN	No	USB_INTPHY_N	USB host or device from internal PHY	USB data line -, connected via R96 to expansion connector X11
116	P	-	-	VRTC	Backup Battery for RTC, for 3V cell, power-switch-over is on the module, Can be left floating, if RTC backup not needed.	3V battery connected
117	P	-	-	GND		
118	P	-	-	3.3V_IN	unswitched 3.3V	3.3V to module
119	P	-	-	VLIO	Mobile: Power from Li-Ion Battery Non-Mobile: connected to 3.3V	Delivers either power from Li-Ion battery or 3.3V_IN
120	P	-	-	3.3V_IN	unswitched 3.3V	3.3V to module

3.2. Connector X2

X2	Type	U-Boot	RESET State	A9M9360 Name	A9M9360 Description after U-Boot	Application A9M9750/A9M9360DEV_1
1		-		NC (PCI_INTA#)		
2	P	-		GND		
3		-		NC (PCI_INTC#)		
4		-		NC (PCI_INTB#)		
5		-		NC (PCI_RESET#)		
6		-		NC (PCI_INTD#)		
7		-		NC (PCI_GNT0#)		
8		-		GND		
9		-		NC (PCI_GNT1#)		
10		-		NC (PCI_CLKOUT)		
11		-		NC (PCI_CLKIN)		
12		-		NC (PCI_GNT2#)		
13		-		NC (PCI_GNT3#)		
14	P	-	-	GND		
15		-		NC (PCI_AD30)		
16		-		NC (PCI_REQ0#)		
17		-		NC (PCI_REQ1#)		
18		-		NC (PCI_REQ2#)		
19		-		NC (PCI_REQ3#)		
20		-		NC (PCI_AD31)		
21		-		NC (PCI_AD28)		
22		-		NC (PCI_AD29)		
23		-		NC (PCI_AD26)		
24		-		NC (PCI_AD27)		
25		-		NC (PCI_AD24)		
26		-		NC (PCI_AD25)		
27		-		NC (PCI_IDSEL)		
28		-		NC (PCI_CBE3#)		
29		-		NC (PCI_AD22)		
30		-		NC (PCI_AD23)		
31		-		NC (PCI_AD20)		
32		-		NC (PCI_AD21)		
33		-		NC (PCI_AD18)		
34		-		NC (PCI_AD19)		
35		-		NC (PCI_AD16)		
36		-		NC (PCI_AD17)		
37		-		NC (PCI_FRAME#)		
38		-		NC (PCI_CBE2#)		
39		-		NC (PCI_TRDY#)		
40		-		GND		
41		-		NC (PCI_IRDY#)		
42		-		NC (PCI_STOP#)		
43		-		NC (PCI_PAR)		
44		-		NC (PCI_DEVSEL#)		
45		-		NC (PCI_AD15)		
46		-		NC (PCI_PERR#)		
47		-		NC (PCI_AD13)		
48		-		NC (PCI_SERR#)		
49		-		NC (PCI_AD11)		
50		-		NC (PCI_CBE1#)		
51		-		NC (PCI_AD9)		
52		-		NC (PCI_AD14)		
53		-		NC (PCI_CBE0#)		
54				NC (PCI_AD12)		
55				NC (PCI_AD6)		
56				NC (PCI_AD10)		
57				NC (PCI_AD4)		
58				NC (PCI_AD8)		
59				NC (PCI_AD2)		
60				NC (PCI_AD7)		
61				NC (PCI_AD5)		
62				NC (PCI_AD3)		
63				NC (PCI_AD1)		
64				NC (PCI_AD0)		
65				NC (LCD_CLKIN)		

X2	Type	U-Boot	RESET State	A9M9360 Name	A9M9360 Description after U-Boot	Application A9M9750/A9M9360DEV_1
66	I	Eth		ETH_TPIN	Ethernet Input-, 100R differential termination on module	Connected to RJ45 with integrated magnetics
67	O	Eth		ETH_LEDLNK	Ethernet Line/Activity LED High, when link ok Low, while active.	Connected to Link/Activity LED in RJ45, needs 100R resistor on application
68	I	Eth		ETH_TPIP	Ethernet Input+, 100R differential termination on module	Connected to RJ45 with integrated magnetics
69	O	Eth		ETH_LEDH	Ethernet High Speed LED High, when 100MB Low, when 10MB	Connected to Speed LED in RJ45, needs 100R resistor on application
70	O	Eth		ETH_TPON	Ethernet Output-, 100R differential termination on module	Connected to RJ45 with integrated magnetics
71	I	Eth		ETH_ESD0	Connected via 0R to Gnd on module	not used
72	O	Eth		ETH_TPOP	Ethernet 0 Output+, 100R differential termination on module	Connected to RJ45 with integrated magnetics
73	P	-		NC (reserved for ETH_EREF)		
74	-	-	-	NC	R/B#, SmartMedia not supported in future, do not connect	
75	-	-		NC	FWE#, SmartMedia not supported in future, do not connect	
76	-	-		NC	FWE#, SmartMedia not supported in future, do not connect	
77	-	-		NC	FCEEXT#, SmartMedia not supported in future, do not connect	
78	-	-		NC	ALE, SmartMedia not supported in future, do not connect	
79	-	-		NC	CLE, SmartMedia not supported in future, do not connect	
80	P	-		GND		
81	I/O	D0		D0	Data Bus	Connected to FPGA U17 and CPLD U2
82	I/O	D1		D1		Connected to FPGA U17 and CPLD U2
83	I/O	D2		D2		Connected to FPGA U17 and CPLD U2
84	I/O	D3		D3		Connected to FPGA U17 and CPLD U2
85	I/O	D4		D4		Connected to FPGA U17 and CPLD U2
86	I/O	D5		D5		Connected to FPGA U17 and CPLD U2
87	I/O	D6		D6		Connected to FPGA U17 and CPLD U2
88	I/O	D7		D7		Connected to FPGA U17 and CPLD U2
89	I/O	D8		D8		Connected to FPGA U17
90	I/O	D9		D9		Connected to FPGA U17
91	I/O	D10		D10		Connected to FPGA U17
92	I/O	D11		D11		Connected to FPGA U17
93	I/O	D12		D12		Connected to FPGA U17
94	I/O	D13		D13		Connected to FPGA U17
95	I/O	D14		D14		Connected to FPGA U17
96	I/O	D15		D15		Connected to FPGA U17
97	I/O	D16		D16		Connected to FPGA U17
98	I/O	D17		D17		Connected to FPGA U17
99	I/O	D18		D18		Connected to FPGA U17
100	I/O	D19		D19		Connected to FPGA U17
101	I/O	D20		D20		Connected to FPGA U17
102	I/O	D21		D21		Connected to FPGA U17
103	I/O	D22		D22		Connected to FPGA U17
104	I/O	D23		D23		Connected to FPGA U17
105	I/O	D24		D24		Connected to FPGA U17
106	I/O	D25		D25		Connected to FPGA U17
107	I/O	D26		D26		Connected to FPGA U17
108	I/O	D27		D27		Connected to FPGA U17

X2	Type	U-Boot	RESET State	A9M9360 Name	A9M9360 Description after U-Boot	Application A9M9750/A9M9360DEV_1
109	I/O	D28		D28		Connected to FPGA U17
110	I/O	D29		D29		Connected to FPGA U17
111	I/O	D30		D30		Connected to FPGA U17
112	I/O	D31		D31		Connected to FPGA U17
113	-	-	-	NC (reserved for A28)		
114	-	-	-	NC (reserved for A29)		
115	-	-	-	NC (reserved for A30)		
116	-	-	-	NC (reserved for A31)		
117	-	-	-	NC (reserved for CANTXD/CANH)		
118	-	-	-	NC (reserved for CANRXD/CANL)		
119	O	CLKOUT	No	BCLKOUT	Clock output, buffered CLKOUT signal, 88.4736MHz	Connected as BCLKOUT to FPGA U17
120	P	-		GND		