NetSilicon
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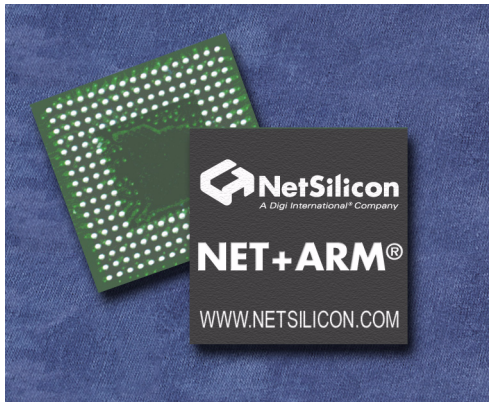
NS7520 Data Sheet

The NetSilicon™ **NS7520** is a high-performance, highly integrated, 32-bit system-on-a chip ASIC designed for use in intelligent networked devices and Internet appliances. The NS7520 is based on the standard architecture in the **NET+ARM**™ family of devices.



The NS7520 can support most any networking scenario, and includes a 10/100 BaseT Ethernet MAC and two independent serial ports (each of which can run in UART, HDLC, or SPI mode).

The CPU is an ARM7TDMI 32-bit RISC processor core with a rich complement of support peripherals and memory controllers for various types of memory (including Flash, SDRAM, EEPROM, and others), programmable timers, a 13-channel DMA controller, an external bus expansion module, and 16 general-purpose input/output (GPIO) pins.

NET+ARM is the hardware foundation for the **NET+Works**™ family of integrated hardware and software solutions for device networking. These comprehensive platforms include drivers, popular operating systems, networking software, development tools, APIs, and complete development boards.

Contents

NS7520 Overview

Figure 1 shows the NS7520 modules. Dashed lines indicate shared pins.

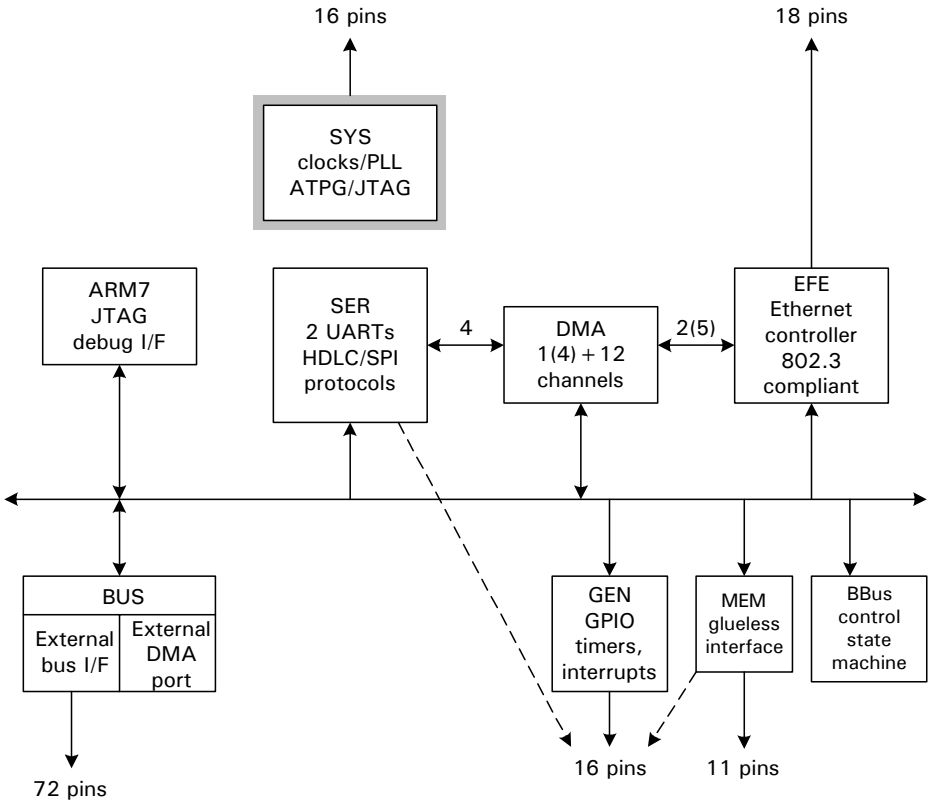


Figure 1: NS7520 modules

Key Features

Table 1 lists the key features of the NS7520.

CPU core

- ARM7TDMI 32-bit RISC processor
- 32-bit internal bus
- 32-bit ARM and 16-bit Thumb mode
- 15 general purpose 32-bit registers
- 32-bit program counter (PC) and status register
- Five supervisor modes, one user mode

Integrated 10/100 Ethernet MAC

- 10/100 Mbps MII-based PHY interface
- 10 Mbps ENDEC interface
- TP-PMD and fiber-PMD device support
- Full-duplex and half-duplex modes
- Optional 4B/5B coding
- Full statistics gathering (SNMP and RMON)
- Station, broadcast, and multicast address detection
- 512-byte transmit FIFO, 2 Kbyte receive FIFO
- Intelligent receive-side buffer selection

13-Channel DMA controller

- Two channels dedicated to Ethernet transmit and receive
- Four channels dedicated to two serial modules' transmit and receive
- Four channels for external peripherals. Only two channels — either 3 and 5 or 4 and 6 — can be configured at one time.
- Three channels available for memory-to-memory transfers
- Flexible buffer management

Programmable Timers

- Two independent timers (2µs–20.7 hours)
- Watchdog timer (interrupt or reset on expiration)
- Programmable bus monitor or timer

General purpose I/O pins

- 16 programmable GPIO interface pins
- 4 pins programmable with level-sensitive interrupt

Operating frequency

- 36, 46, or 55 MHz internal clock operation from 18.432 MHz crystal
- f_{MAX} = 36, 46, or 55 (grade–dependent)
- System clock source by external crystal or clock signal
- Programmable PLL, which allows a range of operating frequencies from 10 to f_{MAX}
- Maximum operating frequency from external clock or using PLL multiplication f_{MAX}

Table 1: NS7520 key features

Serial ports

- Two fully independent serial ports (UART, HDLC, SPI)
- Digital phase lock loop (DPLL) for receive clock extractions
- 32-byte transmit/receive FIFOs
- Internal programmable bit-rate generators
- Bit rates 75–230400 in 16X mode
- Bit rates 1200 bps–4 Mbps in 1X mode
- Flexible baud rate generator, external clock for synchronous operation
- Receive-side character and buffer gap timers
- Four receive-side data match detectors

Bus interface

- Five independent programmable chip selects with 256 Mb addressing per chip select
- Chip select support for SRAM, FP/EDO DRAM, SDRAM, Flash, and EEPROM without external glue
- 8-, 16-, and 32-bit peripheral support
- External address decoding and cycle termination
- Dynamic bus sizing
- Internal DRAM/SDRAM controller with address multiplexer and programmable refresh frequency
- Internal refresh controller (CAS before RAS)
- Burst-mode support
- 0–63 wait states per chip select
- Bootstrap support

Power and Operating Voltages

- 508 mW maximum at 55 MHz (all outputs switching)
- 425 mW maximum at 46 MHz (all outputs switching)
- 333 mW maximum at 36 MHz (all outputs switching)
- 3.3 V — I/O
- 1.5 V — Core

Table 1: NS7520 key features

Operating frequency

The NS7520 is available in grades operating at three speeds: 36 MHz, 46 MHz, and 55 MHz. The operating frequency is set during bootstrap initialization, using pins A[8:1]. These address pins load the PLL Settings register on powerup reset. A[8:7} determines IS (charge pump current); A[6:5] determines FS (output divider), and A[4:1] defines ND (PLL multiplier). Each bit in A[8:1] can be set individually. To set the operating frequency, add a pulldown resistor to the appropriate A[*n*] bit:

Speed	Modify	Resulting IS value		Resulting ND value				
55 MHz	Leave each pin as is	1	0	0	1	0	1	1
46 MHz	Add a pulldown resistor to A[1], to change the value from 1 to 0	1	0	0	1	0	0	1
36 MHz	Add pulldown resistors to A[3:2]	1	0	0	0	1	1	1

Table 2: Operating frequency

Packaging and pinout

Table 3 provides the NS7520 packaging dimensions. Figure 2 shows the NS7520 pinout and dimensions.

Symbol	Min	Nom	Max
A	—	—	1.4
A1	0.35	0.40	0.45
A2	—	—	0.95
b	0.45	0.50	0.55
D		13.0 BSC	
D1		11.2 BSC	
E		13.0 BSC	
E1		11.2 BSC	
e		0.8 BSC	
aaa		0.1	

Table 3: NS7520 packaging dimensions

177 PFBGA

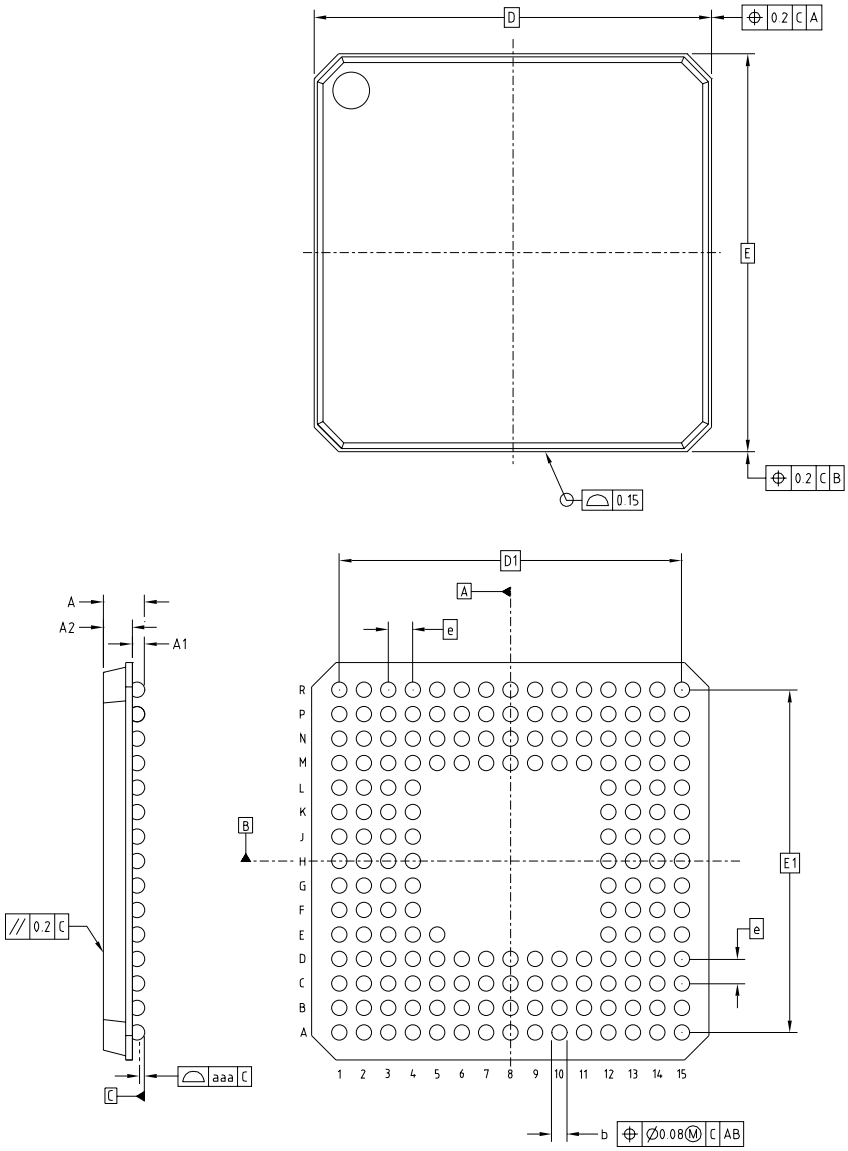


Figure 2: NS7520 pinout and dimensions

Pinout detail tables

Each pinout table applies to a specific interface and contains the following information:

Signal	The pin name for each I/O signal. Some signals have multiple function modes and are identified accordingly. The mode is configured through firmware using one or more configuration registers.
Pin	The pin number assignment for a specific I/O signal. ■ **U** next to the pin number indicates that the pin is a pullup resistor. ■ **D** next to the pin number indicates that the pin is a pulldown resistor. ■ **No value** next to the pin indicates that the pin has neither a pullup nor pulldown resistor. See Figure 6, "Internal pullup characteristics," on page 21 and Figure 7, "Internal pulldown characteristics," on page 21 for an illustration of the characteristics of these pins. Use the figures to select the appropriate value of the complimentary resistor to drive the signal to the opposite logic state. For those pins with no pullup or pulldown resistor, you must select the appropriate value per your design requirements.
_	An underscore (bar) indicates that the pin is *active low*.
I/O	The type of signal — input, output, or input/output.
OD	The output drive strength of an output buffer. The NS7520 uses one of three drivers: ■ 2 mA ■ 4 mA ■ 8 mA

Notes:

- NO CONNECT as a pin description means *do not connect to this pin*.
- The 177th pin (package ball is for alignment of the package on the PCB.

System Bus interface

Symbol		Pin	I/O	OD	Description	
BCLK		A6	0	8	Synchronous bus clock	
External bus	**Other**				**External bus**	**Other**
ADDR27	CS0OE_	N10 U	I/O	4	Addr bit 27	Logical AND of CS0_ and OE_
ADDR26	CS0WE_	P10 U	I/O	4	Addr bit 26	Logical AND of CS_ and WE_
External bus					**External bus**	
ADDR25		M10 U	I/O	4	Remainder of address bus (through ADDR0)	
ADDR24		R10 U	I/O	4		
ADDR23		N9 U	I/O	4		
ADDR22		R9 U	I/O	4		
ADDR21		M9 U	I/O	4		

Symbol	Pin	I/O	OD	Description
ADDR20	N8 U	I/O	4	
ADDR19	P8 U	I/O	4	
ADDR18	M7 U	I/O	4	
ADDR17	R7 U	I/O	4	
ADDR16	N7 U	I/O	4	
ADDR15	R6 U	I/O	4	
ADDR14	M6 U	I/O	4	
ADDR13	P6 U	I/O	4	
ADDR12	N6 U	I/O	4	
ADDR11	M5 U	I/O	4	
ADDR10	P5 U	I/O	4	
ADDR9	N5 U	I/O	4	
ADDR8	R4 U	I/O	4	
ADDR7	R3 U	I/O	4	
ADDR6	R2 U	I/O	4	
ADDR5	M4 U	I/O	4	
ADDR4	N4 U	I/O	4	
ADDR3	R1 U	I/O	4	
ADDR2	M3 U	I/O	4	
ADDR1	N2 U	I/O	4	
ADDR0	P1 U	I/O	4	
DATA31	N1	I/O	4	Data bus
DATA30	M1	I/O	4	
DATA29	L3	I/O	4	
DATA28	L2	I/O	4	
DATA27	L4	I/O	4	
DATA26	L1	I/O	4	
DATA25	K3	I/O	4	
DATA24	K2	I/O	4	
DATA23	K1	I/O	4	
DATA22	J2	I/O	4	
DATA21	J3	I/O	4	
DATA20	J1	I/O	4	

Symbol	Pin	I/O	OD	Description
DATA19	H3	I/O	4	
DATA18	H4	I/O	4	
DATA17	H1	I/O	4	
DATA16	H2	I/O	4	
DATA15	G4	I/O	4	
DATA14	G1	I/O	4	
DATA13	G3	I/O	4	
DATA12	G2	I/O	4	
DATA11	F4	I/O	4	
DATA10	F2	I/O	4	
DATA9	F3	I/O	4	
DATA8	E1	I/O	4	
DATA7	E2	I/O	4	
DATA6	E3	I/O	4	
DATA5	D1	I/O	4	
DATA4	C1	I/O	4	
DATA3	B1	I/O	4	
DATA2	D4	I/O	4	
DATA1	D3	I/O	4	
DATA0	C2	I/O	4	
BE3_	D9	I/O	2	Byte enable D31:D24
BE2_	A9	I/O	2	Byte enable D23:D16
BE1_	C9	I/O	2	Byte enable D15:D08
BE0_	B9	I/O	2	Byte enable D07:D00
TS_	A8	I/O	4	DO NOT USE Add an external 820 ohm pullup to 3.3 V.
TA_	D8 U	I/O	4	Data transfer acknowledge Add an external 820 ohm pullup to 3.3 V. TA_ is bidirectional. It is used in input mode to terminate a memory cycle externally. It is used in output mode for reference purposes only.
TEA_	C8 U	I/O	4	Data transfer error acknowledge Add an external 820 ohm pullup to 3.3 V. TEA_ is bidirectional. It is used in input mode to terminate a memory cycle externally. It is used in output mode for reference purposes only.

Symbol	Pin	I/O	OD	Description
RW_	D6	I/O	2	Transfer direction
BR_	D7	NO CONNECT		
BG_	C7	NO CONNECT		
BUSY_	B7	NO CONNECT		

Chip select controller

The NS7520 supports five unique chip select configurations.

Symbol	Pin	I/O	OD	Description
CS4_	B4	O	4	Chip select/DRAM RAS_
CS3_	A4	O	4	Chip select/DRAM RAS_
CS2_	C5	O	4	Chip select/DRAM RAS_
CS1_	B5	O	4	Chip select/DRAM RAS_
CS0_	D5	O	4	Chip select (boot select)
CAS3_	A1	O	4	FP/EDO DRAM column strobe D31:D24/SDRAM RAS_
CAS2_	C4	O	4	FP/EDO DRAM column strobe D23:D16/SDRAM CAS_
CAS1_	B3	O	4	FP/EDO DRAM column strobe D15:D08/SDRAM WE_
CAS0_	A2	O	4	FP/EDO DRAM column strobe D07:D00/SDRAM A10(AP)
WE_	C6	O	4	Write enable for NCC Ctrl'd cycles
OE_	B6	O	4	Output enable for NCC Ctrl'd cycles

Ethernet interface MAC

Note: ENDEC values for general-purpose output and TXD refer to bits in the Ethernet General Control register. ENDEC values for general-purpose input and RXD refer to bits in the Ethernet General Status register.

In this table, *GP* designates *general-purpose*.

Symbol		Pin	I/O	OD	Description	
MII	**ENDEC**				**MII**	**ENDEC**
MDC	GP output	D10	O	2	MII management clock	State of (LPBK bit XOR (Mode = SEEQ))
MDIO	GP output	B10 U	I/O	2	MII data	State of UTP_STP bit
TXCLK		C10	I		TX clock	
TXD3	GP output	A12	O	2	TX data 3	State of AUI_TP[0] bit

Symbol		Pin	I/O	OD	Description	
TXD2	GP output	B11	O	2	TX data 2	State of AUI_TP[1] bit
TXD1	GP output	D11	O	2	TX data 1	Inverted state of PDN bit, open collector
TXD0	TXD	A11	O	2	TX data 0	Transmit data
TXER	GP output	A13	O	2	TX code err	State of LNK_DIS_ bit
TXEN		B12	O	2	TX enable	
TXCOL		A14	I		Collision	
RXCRS		D12	I		Carrier sense	
RXCLK		C12	I		RX clock	
RXD3	GP input	D14	I		RX data 3	Read state in bit 12
RXD2	GP input	B15	I		RX data 2	Read state in bit 15
RXD1	GP input	A15	I		RX data 1	Read state in bit 13
RXD0	RXD	B13	I		RX data 0	Receive data
RXER	GP input	C15	I		RX error	Read state in bit 11
RXDV	GP input	D15	I		RX data valid	Read state in bit 10

"No connect" pins

Pin	Description
R13	Add a 15K ohm pulldown to GND (15K ohm is the recommended value; 10–20K ohms is acceptable)
P12	Add a 15K ohm pulldown to GND (15K ohm is the recommended value; 10–20K ohms is acceptable)
N12	Tie to GND
R15	XTALB2: NO CONNECT
M11	NO CONNECT
P11	NO CONNECT
N11	NO CONNECT
R12	NO CONNECT
R14	NO CONNECT
P13	NO CONNECT

Note: If your design implements 10–20K ohm *pullups* instead of *pulldowns* on R13 and P12, and a pullup on N12 instead of *GND*, no further action is required.

General Purpose I/O

GPIO signal	Serial signal	Other signal	Pin	I/O	OD	Serial channel description	Other description
PORTA7	TXDA		J14 U	I/O	2	Channel 1 TXD	
PORTA6	DTRA_	DREQ1_	J13 U	I/O	2	Channel 1 DTR_	DMA channel 3/5 Req
PORTA5	RTSA_		J15 U	I/O	2	Channel 1 RTS_	
PORTA4	RXCA/RIA_/ OUT1A_		J12 U	I/O	2	Pgm'able Out/ Channel 1 RXCLK/ Channel 1 ring signal/ Channel 1 SPI clock (CLK)	
PORTA3	RXDA	DACK1_	H15 U	I/O	2	Channel 1 RXD	DMA channel 3/5 ACK
PORTA2	DSRA_	AMUX	H12 U	I/O	2	Channel 1 DSR_	DRAM addr mux
PORTA1	CTSA_	DONE1_ (O)	H13 U	I/O	2	Channel 1 CTS_	DMA channel 3/5 DONE_Out
PORTA0	TXCA/ OUT2A_/ DCDA_	DONE1_ (I)	G12 U	I/O	2	Pgm'able Out/ Channel 1 DCD/ Channel 1 SPI enable (SEL_)/ Channel 1 TXCLK	DMA channel 3/5 DONE_In
PORTC7	TXDB		G13 U	I/O	2	Channel 2 TXD	GEN interrupt out
PORTC6	DTRB_	DREQ2_	G14 U	I/O	2	Channel 2 DTR_	DMA Channel 4/6 Req
PORTC5	RTSB_	REJECT_	F15 U	I/O	2	Channel 2 RTS_	CAM reject
PORTC4	RXCB/RIB_/ OUT1B_	RESET_	F12 U	I/O	2	Pgm'able Out/ Channel 2 RXCLK/Channel 2 ring signal/ Channel 2 SPI clock (CLK)	RESET output
PORTC3*	RXDB	LIRQ3/ DACK2_	F13 U	I/O	2	Channel 2 RXD	Level sensitive IRQ / DMA channel 4/6 ACK
PORTC2*	DSRB_	LIRQ2/RPSF_	E15 U	I/O	2	Channel 2 DSR_	Level sensitive IRQ/ CAM request
PORTC1*	CTSB_	LIRQ1/ DONE2_(O)	E12 U	I/O	2	Channel 2 CTS_	Level sensitive IRQ / DMA channel 4/6 DONE_Out

GPIO signal	Serial signal	Other signal	Pin	I/O	OD	Serial channel description	Other description
PORTC0*	TXCB/ OUT2B_/ DCDB_	LIRQ0/ DONE2_(I)	E14 U	I/O	2	Pgm'able Out/ Channel 2 DCD/ Channel 2 SPI enable (SEL_)/ Channel 2 TXCLK	Level sensitive IRQ / DMA channel 4/6 DONE_In

* PORTC[3:0] pins provide level-sensitive interrupts. The inputs do not need to be synchronous to any clock. The interrupt remains active until cleared by a change in the input signal level.

System clock and reset

Symbol	Pin	I/O	OD	Description
XTALA1	K14	I		ARM/system oscillator circuit
XTALA2	K12	O		
PLLVDD (1.5V)	L15	P		PLL clean power
PLLVSS	L12	P		PLL return
RESET_	A10	I		System reset

System mode (test support)

PLLTST_, BISTEN_, and SCANEN_ primary inputs control different test modes for both functional and manufacturing test operations (see Table 4: "NS7520 test modes" on page 18).

Symbol	Pin	I/O	OD	Description
PLLTST_	N15	I		Encoded with BISTEN_ and SCANEN_ Add an external pullup to 3.3V or pulldown to GND.
BISTEN_	M15	I		Encoded with PLLTST_ and SCANEN_ Add an external pullup to 3.3V or pulldown to GND.
SCANEN_	L13	I		Encoded with BISTEN_ and PLLTST_ Add an external pullup to 3.3V or pulldown to GND. See "System (SYS) module," beginning on page 14, for additional information about SCANEN_.

JTAG test

JTAG boundary scan allows a tester to check the soldering of all signal pins and tri-state all outputs.

Symbol	Pin	I/O	OD	Description
TDI	N14 U	I		Test data in.

Symbol	Pin	I/O	OD	Description
TDO	M13	O	2	Test data out.
TMS	M12 U	I		Test mode select.
TRST_	M14	I		Test mode reset. Requires external termination when not being used (see Figure 3, "TRST_ termination," on page 13 for an illustration of the termination circuit on the development PCB).
TCK	P15	I		Test mode clock. Add an external pullup to 3.3V.

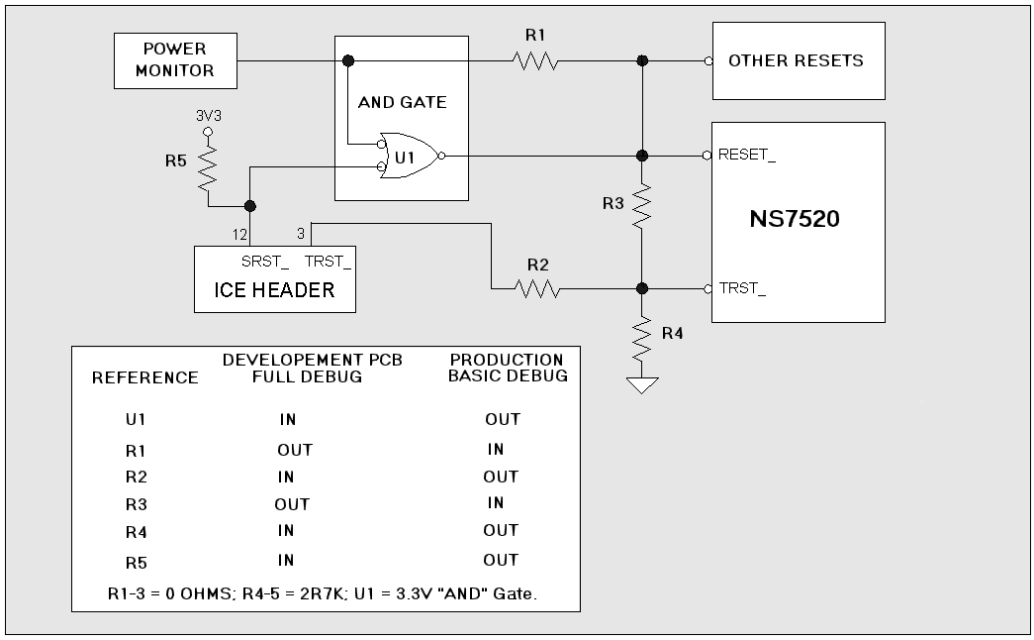


Figure 3: TRST_ termination

Power supply

Signal	Pin	Description
Oscillator VCC (3.3V)	N13, C3	Oscillator power supply
Core VCC (1.5V)	R8, L14, C14, C13	Core power supply
I/O VCC (3.3V)	E4, K4, M2, N3, P3, R5, H14, F14, B8, A3	I/O power supply
GND	D2, F1, J4, P4, P7, M8, P9, R11, K15, G15, E13, D13, B14, C11, A7, A5, B2, P2, P14, K13	Ground

NS7520 modules

CPU module

The CPU uses an ARM7TDMI core processor. The ARM architecture is based on Reduced Instruction Set Computer (RISC) principles, which result in high instruction throughput and impressive real-time interrupt response for a small, cost-effective circuit. For more information about ARM7TDMI, see the ARM7TDMI Data Sheet from ARM Ltd. (www.arm.com).

GEN module

The GEN module provides the NS7520 with its main system control functions, as well as these features:

- Two programmable timers with interrupt
- One programmable bus-error timer
- One programmable watchdog timer
- Two 8-bit programmable general-purpose I/O ports

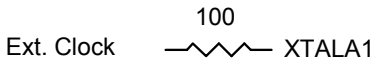
System (SYS) module

The system module provides the system clock (SYS_CLK) and system reset (SYS_RESET) resources. The IO_XTALA clock is generated in one of two ways:

- By tying an external crystal or ceramic resonator to the XTALA*n* pins and using the internal oscillator.
- By feeding a clock directly to the XTALA1 pin.

When using an external crystal or ceramic resonator to drive the clock signal, review the electrical specifications for recommended crystal or ceramic resonator and external component characteristics.

When using an external clock to drive the clock signal, use this circuit (required):



$F_{CRYSTAL}$ is defined as the frequency of the crystal or ceramic resonator and the output frequency of the oscillator. The IO_XTALA signal is fed to or through an internal phase locked loop, depending on the state of {PLLTST_, BISTEN_, SCANEN_}. The NS7520 ARM processor and system interface logic operate off the SYS_CLK signal. The frequency of SYS_CLK is $F_{CRYSTAL}$ when the PLL is disabled; otherwise, the frequency is 1/4 the PLL frequency.

Note: When configured to use the internal PLL clock generator, the NS7520 system clock might initialize to 1/2 the configured frequency. To ensure that the PLL state machine drives to a correct state, invert the RESET_ signal and apply it to the SCANEN_ pin. The maximum delay (inverter propagation delay plus PCB etch delay) between pins A10 and L13 must be less than 8 ns, as shown in Figure 4:

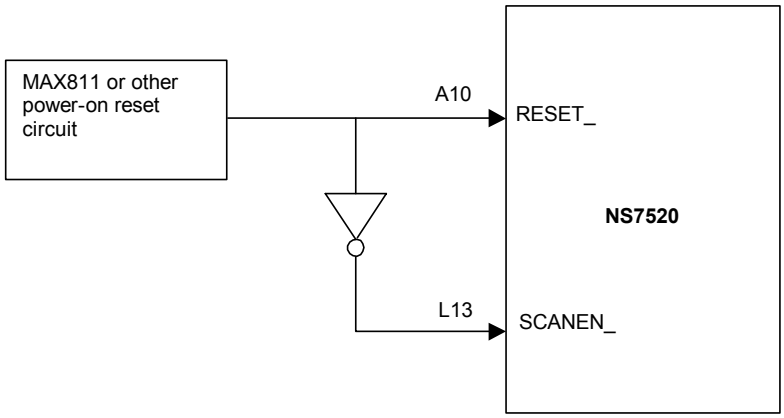


Figure 4: NS7520 clock speed with maximum delay

BBus module

The BBus module provides the data path among NS7520 internal modules. This module provides the address and data multiplexing logic that supports the data flow through the NS7520. The BBus module is the central arbiter for all the NS7520 bus masters and, once mastership is granted, handles the decoding of each address to one (or none) of the NS7520 modules.

Memory module (MEM)

The memory module provides a glueless interface to external memory devices such as Flash, DRAM, and EEPROM. The memory controller contains an integrated DRAM controller and supports five unique chip select configurations.

The memory module monitors the BBus interface for access to the bus module; that is, any access not addressing internal resources. If the address to be used corresponds to a Base Address register in the memory module, the memory module provides the memory access signals and responds to the BBus with the necessary completion signal.

The memory module can be configured to interface with FP, EDO, or SDRAM (synchronous DRAM), although the NS7520 cannot interface with more than one device type at a time.

DMA controller

The NS7520 contains one DMA controller, with 13 DMA channels. Each DMA channel moves blocks of data between memory and a memory peripheral.

The DMA controller supports both fly-by operations and memory-to-memory operations:

- When configured for fly-by operation, the DMA controller transfers data between one of the NS7520 peripherals and a memory location.
- When configured for memory-to-memory operations, the DMA controller uses a temporary holding register between read and write operations. Two memory cycles are executed.

Ethernet controller

The Ethernet controller provides the NS7520 with one IEEE 802.3u compatible Ethernet interface. The Ethernet interface includes the Ethernet front-end (EFE) and media access controller (MAC).

The Ethernet module supports both media independent interface (MII) and ENDEC modes.

The MAC module interfaces to an external physical layer (PHY) device using the MII standard defined by IEEE 802.3u. The MAC interface includes the MII clock and data signals.

Figure 5 shows a high-level block diagram of the EFE module, which provides the FIFO handling interface between the NS7520 BBus and the MAC modules.

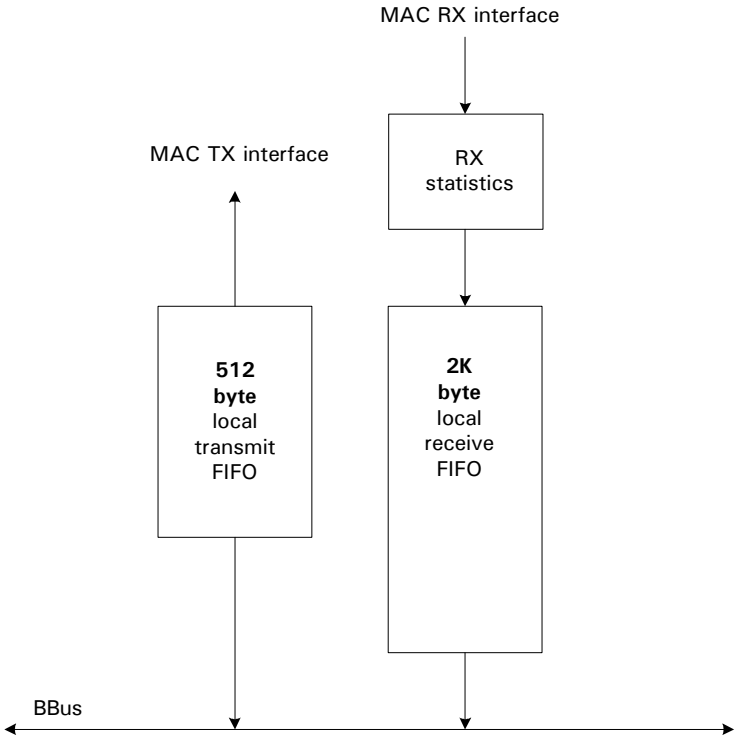


Figure 5: EFE module block diagram

Serial controller

The NS7520 supports two independent universal asynchronous/synchronous receiver/transmitter channels. Each channel supports these features:

- Independent programmable bit-rate generator
- UART, HDLC, SPI (master) modes
- High-speed data transfer:
  - x1 mode: 4Mbits/sec
  - x16 mode: 230 Kbits/sec
- 32–byte TX FIFO
- 32–byte RX FIFO
- Programmable data format: 5–6, 8 data bits; odd, even, or no parity; 1, 2 stop bits
- Programmable channel modes: normal, local loopback, remote loopback
- Control signal support
- Maskable interrupt conditions:
  - Receive break detection
  - Receive framing error
  - Receive parity error
  - Receive overrun error
  - Receive FIFO ready
  - Receive FIFO half-full
  - Transmit FIFO ready
  - Transmit FIFO half-empty
  - CTS, DSR, DCD, RI state change detection
- Clock/data encoding: NRZ, NRZB, NRZI, FM, Manchester
- Multi-drop capable

NS7520 bootstrap initialization

Many internal NS7520 features are configured when the RESET pin is asserted. The address bus configures the appropriate control register bits at powerup. This table shows which bits control which functions:

Address bit	Name	Description
ADDR[27]	Endian configuration	0 Little Endian configuration 1 Big Endian configuration
ADDR[26]	CPU bootstrap	0 CPU disabled; GEN_BUSER = 1 1 CPU enabled; GEN_BUSER = 0
ADDR[24:23]	CS0/MMCR[19:18] setting	00 8-bit SRAM, 63 wait-states/2'b00 01 32-bit SRAM, 63 wait-states/2'b00 10 32-bit SRAM, 63 wait-states/2'b11 11 16-bit SRAM, 63 wait-states/2'b00
ADDR[19:9]	GEN_ID setting	GEN_ID = A[19:09],default = 'h3ff
ADDR[8:7]	PLL IS setting	IS = A[8:7]*xnor'b10*,default = 'b10
ADDR[6:5]	PLL FS setting	FS = A[6:5]*xnor'b00*,default = 'b00
ADDR[4:0]	PLL ND setting	ND = A[4:0]*xnor'd11*,default = 'd11 **Note:** A[0] cannot be pulled down

Table 4: NS7520 test modes

Test modes and PLL operation

The PLLTST_, BISTEN_, and SCANEN_ primary inputs control test modes for both functional and manufacturing test operations. Table 4 shows how these inputs are coded.

{PLLTST_, BISTEN_, SCANEN_}	Conditions	Test modes	Normal operation	JTAG TAP controller
0	Reserved for factory test	N/A	N/A	N/A
1	Reserved for factory test	N/A	N/A	N/A
2	Reserved for factory test	N/A	N/A	N/A
3	All outputs normal function, PLL disabled	None	PLL bypassed using oscillator or external clock	Boundary scan
4	All outputs normal, PLL enabled	None	PLL operational using oscillator or external clock	Boundary scan
5	Reserved for factory test	N/A	N/A	N/A

{PLLTST_, BISTEN_, SCANEN_}	Conditions	Test modes	Normal operation	JTAG TAP controller
6	All outputs normal function, PLL enabled	None	PLL operational using oscillator or external clock	ARM JTAG debugger
7	All outputs normal function, PLL disabled	None	PLL bypassed using oscillator or external clock	ARM JTAG debugger

JTAG

The NS7520 provides full support for 1149.1 JTAG boundary scan testing. All NS7520 pins can be controlled using the JTAG interface port. The JTAG interface provides access to the ARM7TDMI debug module when the appropriate combination of PLLTST_, BISTEN_, and SCANEN_ is selected (as shown in Table 4: "NS7520 test modes").

ARM Debug

The ARM7TDMI core uses a JTAG TAP controller that shares the pins with the TAP controller used for 1149.1 JTAG boundary scan testing. To enable the ARM7TDMI TAP controller, {PLLTST_,BISTEN_,SCANEN_} must be set as shown in Table 4: "NS7520 test modes".

The NS7520 is compatible with two ICE debuggers:

- Macraigor Systems Raven (also called *Blackbird*)
- EPI JEENI probe

Factory-tested

The NS7520 is factory-tested using standard BIST techniques, including flip-flop ATPG chains, internal memory BIST, ARM standard tests for the ARM7TDMI core, and a test isolating the PLL.

DC characteristics and other operating specifications

The NS7520 operates using an internal core V_{DD} supply voltage of 1.5V. A 3.3VC supply is required for the I/O cells, which drive/accept 3.3V levels.

Table 5 provides the DC characteristics for inputs; Table 6 provides the DC characteristics for outputs.

Sym	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}	Input high voltage		2.0		3.6	V
V_{IL}	Input low voltage		V_{SS} – 0.3		0.8	V

Table 5: DC characteristics — inputs

Sym	Parameter	Conditions	Min	Typ	Max	Unit
P	Power consumption	F_{SYSCLK} = 55 MHz			508	mW
		Core			192	mW
		I/O			316	mW
		F_{SYSCLK} = 46 MHz			425	mW
		Core			161	mW
		I/O			264	mW
		F_{SYSCLK} = 36 MHz			333	mW
		Core			126	mW
		I/O			207	mW
V_{OL}	Output low voltage	Outputs & bi-directional	0		0.4	V
V_{OH}	Output high voltage	Outputs & bi-directional	2.4		VCC	V

Table 6: DC characteristics — outputs

Table 7 defines the DC operating (thermal) conditions for the NS7520. Operating the NS7520 outside these conditions results in unpredictable behavior.

Sym	Parameter	Conditions	Min	Typ	Max	Unit
V_{DD}	Core supply voltage		1.4	1.5	1.6	V
V_{CC}	I/O supply voltage		3.0	3.3	3.6	V
T_{OP}	Ambient temperature		-40		85	^{o}C
T_J	Junction temperature			110		^{o}C
T_{STG}	Storage temperature		-40		125	^{o}C
θ_J	Pkg thermal resistance			50		^{o}C/W
I_{IH}	Input threshold	No pullup	-10		10	µA
I_{IL}	Input current as “0”	No pullup	10		10	µA
I_{OZ}	HighZ leakage current	Any input	-10		10	µA
C_{IO}	Pin capacitance	$V_O = 0$			7	pF

Table 7: Recommended operating temperatures

Pad pullup and pulldown characteristics

Figure 6 illustrates characteristics for a pad with internal pullup; Figure 7 illustrates characteristics for a pad with internal pulldown. See "Pinout detail tables," beginning on page 6, for information about which pins use pullup and pulldown resistors.

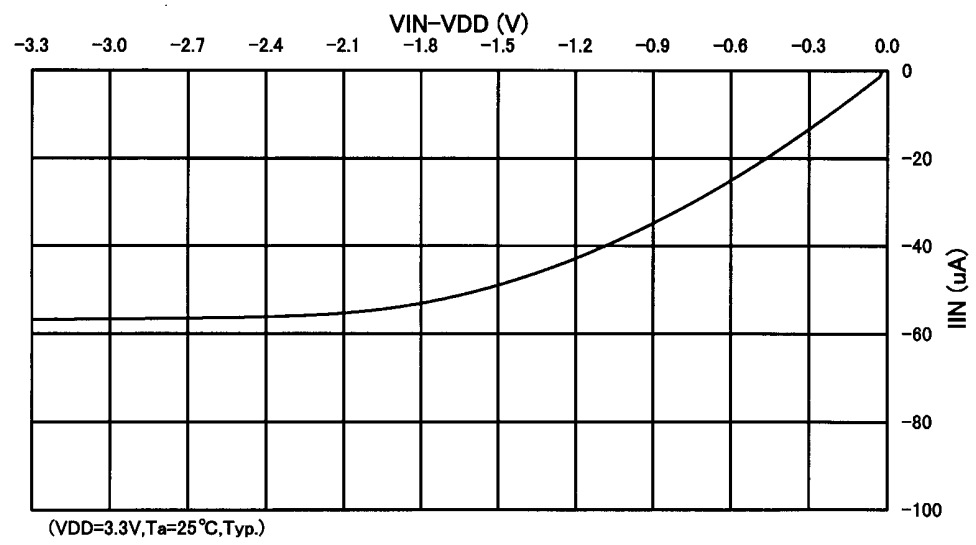


Figure 6: Internal pullup characteristics

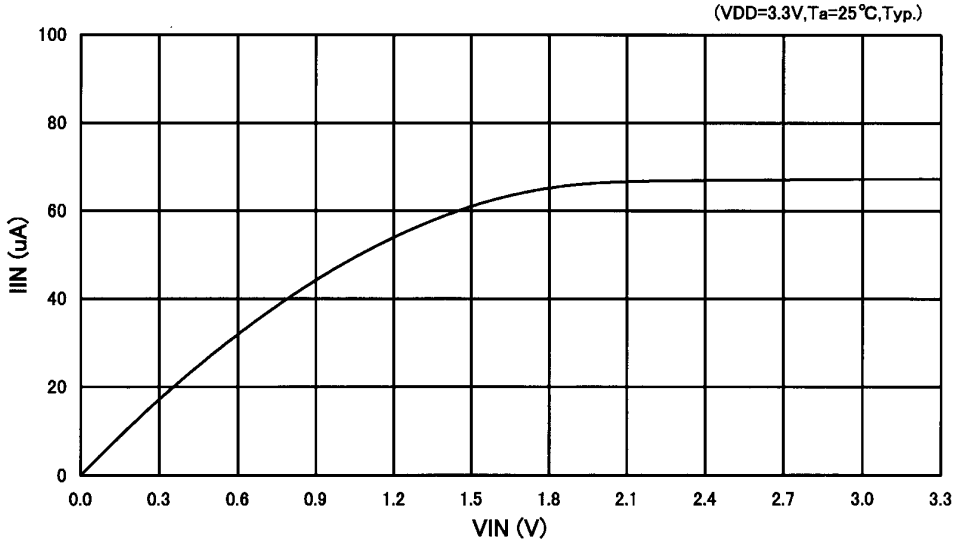


Figure 7: Internal pulldown characteristics

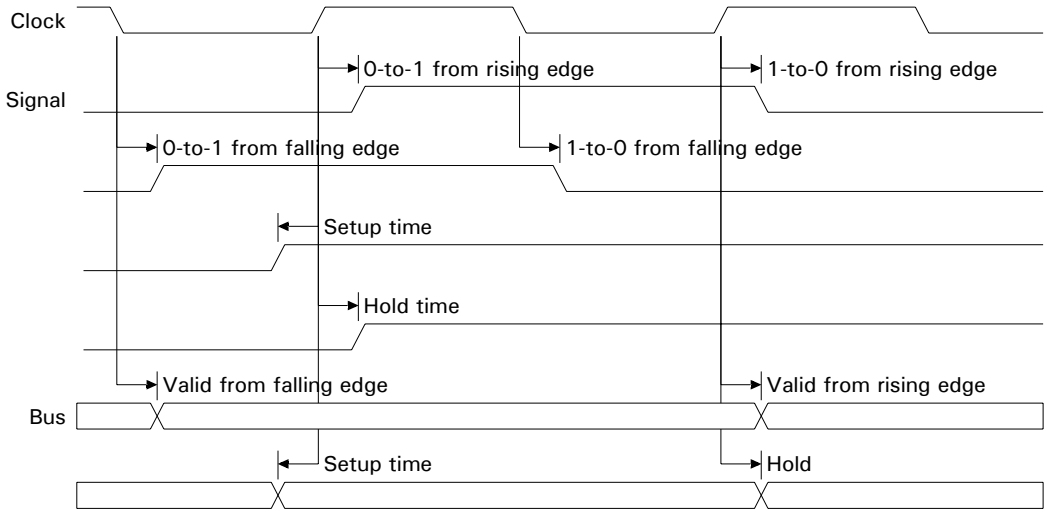
Timing Diagrams

timing_specifications

All timing specifications consist of the relationship between a reference clock and a signal:

- There are bussed and non–bussed signals. Non–bussed signals separately illustrate 0–to–1 and 1–to–0 transitions.
- Inputs have setup/hold times versus clock rising.
- Outputs have switching time relative to either clock rising or clock falling.

Note: Timing relationships in this diagram are drawn without proportion to actual delay.

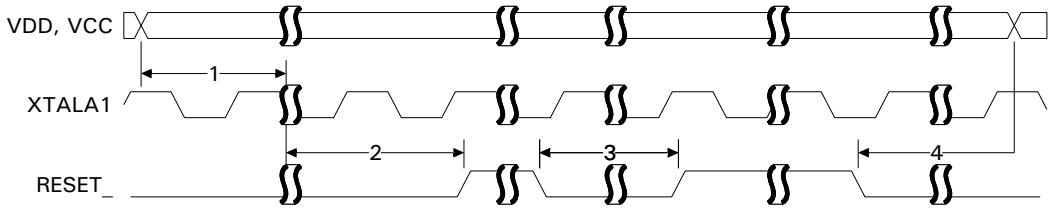


reset_timing

From poweroff, reset must be asserted until all power supplies are above their specified thresholds. An additional 8 microseconds is required for oscillator settling time. After the oscillator is settled and while valid power is maintained, reset must be asserted for three periods of the XTALA1 clock in the following situations:

- Before release of reset after application of power
- While valid power is maintained to initiate *hot reset* (reset while power is at or above specified thresholds)
- Before loss of valid power during power outage/power down

The PORTC4 output indicates the reset state of the chip. PORTC4 persists beyond the negation of RESET_ for approximately 512 system clock cycles if the PLL is disabled. When the PLL is enabled, PORTC4 persists beyond the negation of RESET_ to allow for PLL lock for 100 microseconds times the ratio of the VCO to XTALA.



reset timing parameters

Num	Description	Min	Typ	Max	Units
1	Power valid before reset negated	8			µs
2	Reset asserted after power valid	3			T_{XTALA1}
3	Reset asserted while power valid	3			T_{XTALA1}
4	Reset asserted before power invalid	3			T_{XTALA1}

SRAM timing

BCLK max frequency: 55.296 MHz

Operating conditions:

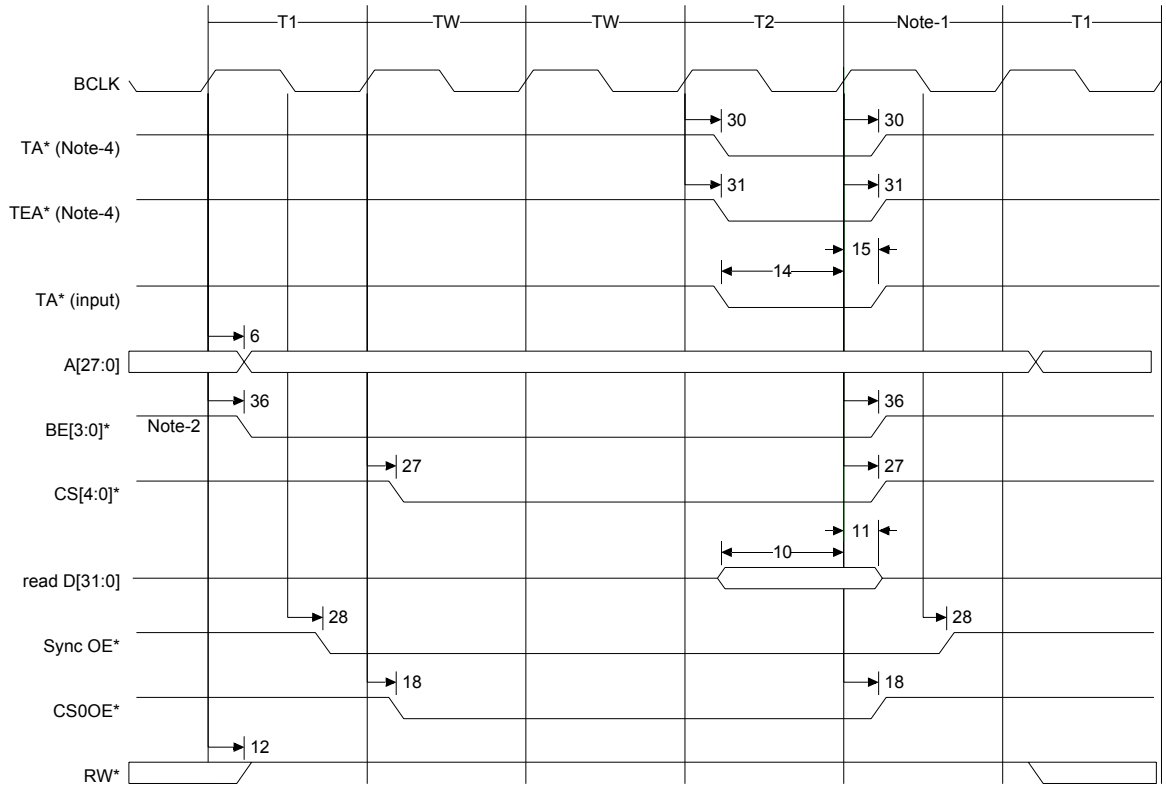
Temperature:	-15.00 (min)	110.00 (max)
Voltage:	1.60 (min)	1.40 (max)
Output load:	25.0pf	
Input drive:	CMOS buffer	

SRAM timing parameters

Num	Description	Min	Max	Unit
36	BCLK high to BE* valid		15.5	ns
6	BCLK high to address valid	5	13.5	ns
9	BCLK high to data out valid		14	ns
13	BCLK high to data out high impedance		13	ns
10	Data in valid to BCLK high (setup)	5		ns
11	BCLK high to data in invalid (hold)	3		ns
14	TA* valid to BCLK high (setup)	5		ns
15	BCLK high to TA* invalid (hold)	3		ns
27	BCLK high to CS* valid		12.5	ns
28	BCLK low to OE* valid		12.5	ns
29	BCLK low to WE* valid		13	ns
30	BCLK high to TA* valid		13.5	ns
31	BCLK high to TEA* valid		16	ns
18	BCLK low to A27 (CS0OE*) valid		13.5	ns
19	BCLK low A26 (CS0WE*) valid		13.5	ns
12	BCLK high to RW* valid		13.5	ns

SRAM read

CS* controlled read (wait = 2)



Notes:

1 If the next transfer is DMA, null periods between memory transfers can occur. Thirteen clock pulses are required for DMA context switching.

2 Port size determines which byte enable signals are active:

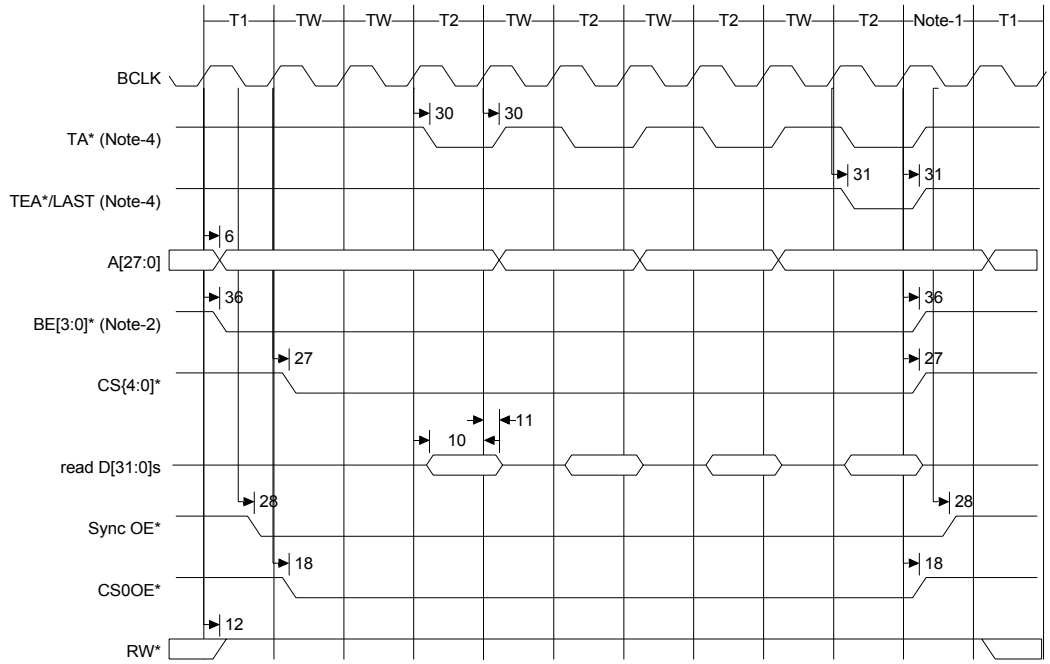
- 8-bit port = BE3*
- 16-bit port = BE[3:0]
- 32-bit port = BE[3:0]

3 The TW cycles are present when the WAIT field is set to 2 or more.

4 The TA* and TEA*/LAST signals are for reference only.

SRAM burst read

CS* controlled, four word (4-2-2-2), burst read (wait = 2, BCYC = 01)



Notes:

1 If the next transfer is DMA, null periods between memory transfers can occur. Thirteen clock pulses are required for DMA context switching.

2 Port size determines which byte enable signals are active:

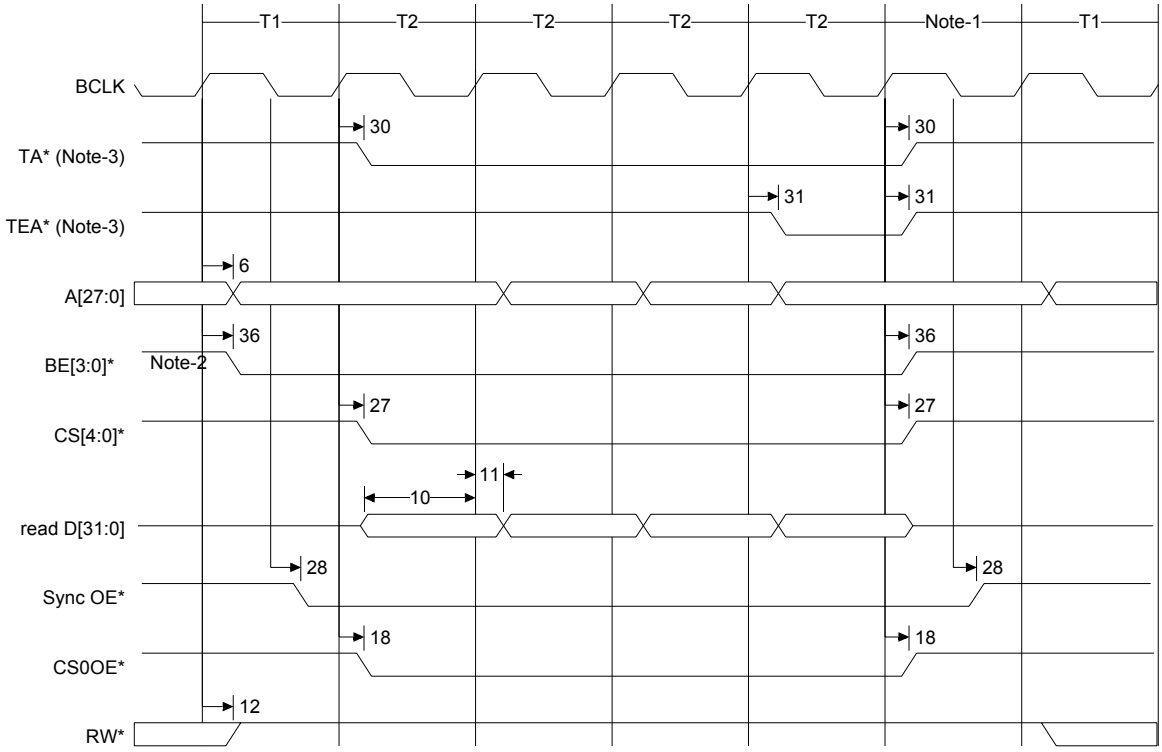
- 8-bit port = BE3*
- 16-bit port = BE[3:0]
- 32-bit port = BE[3:0]

3 The TW cycles are present when the WAIT field is set to 2 or more.

4 The TA* and TEA*/LAST signals are for reference only.

SRAM burst read (2111)

CS* controlled read (wait = 0, BCYC = 00)



Notes:

1 If the next transfer is DMA, null periods between memory transfers can occur. Thirteen clock pulses are required for DMA context switching.

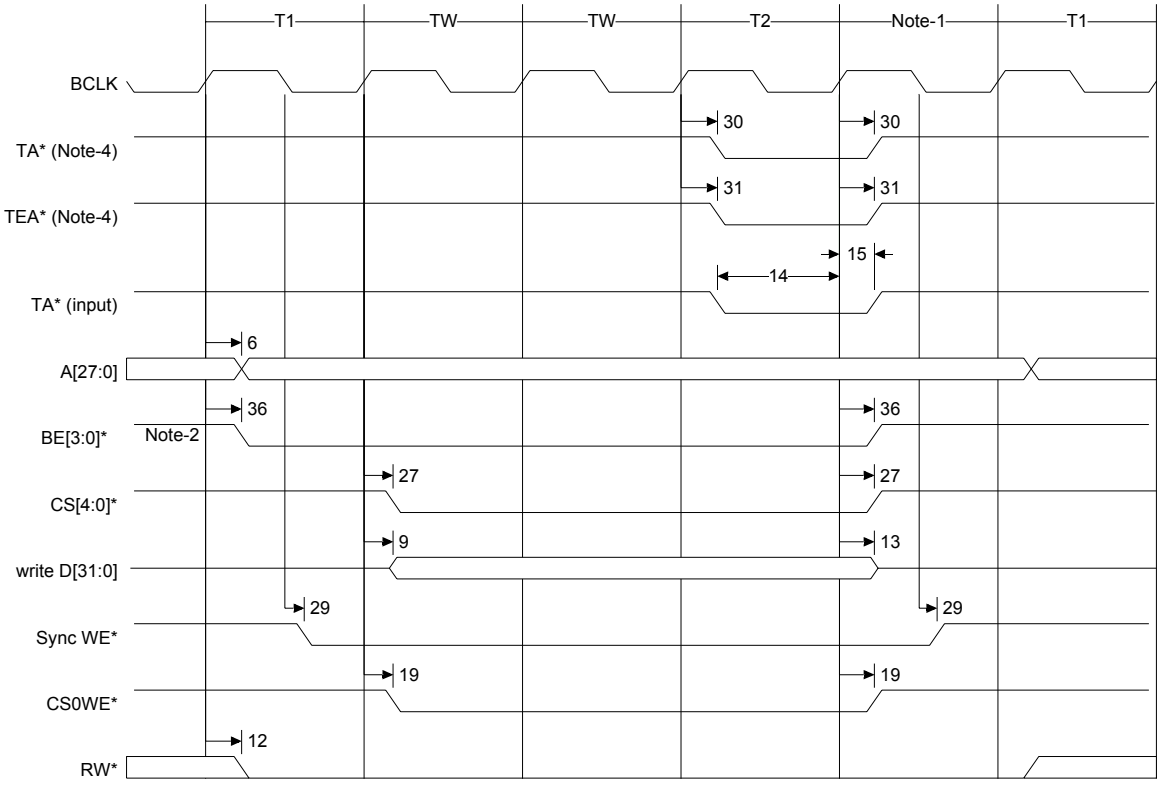
2 Port size determines which byte enable signals are active:

- 8-bit port = BE3*
- 16-bit port = BE[3:0]
- 32-bit port = BE[3:0]

3 The TA* and TEA*/LAST signals are for reference only.

SRAM write

CS controlled write (internal and external), (wait = 2)



Notes:

1 If the next transfer is DMA, null periods between memory transfers can occur. Thirteen clock pulses are required for DMA context switching.

2 Port size determines which byte enable signals are active:

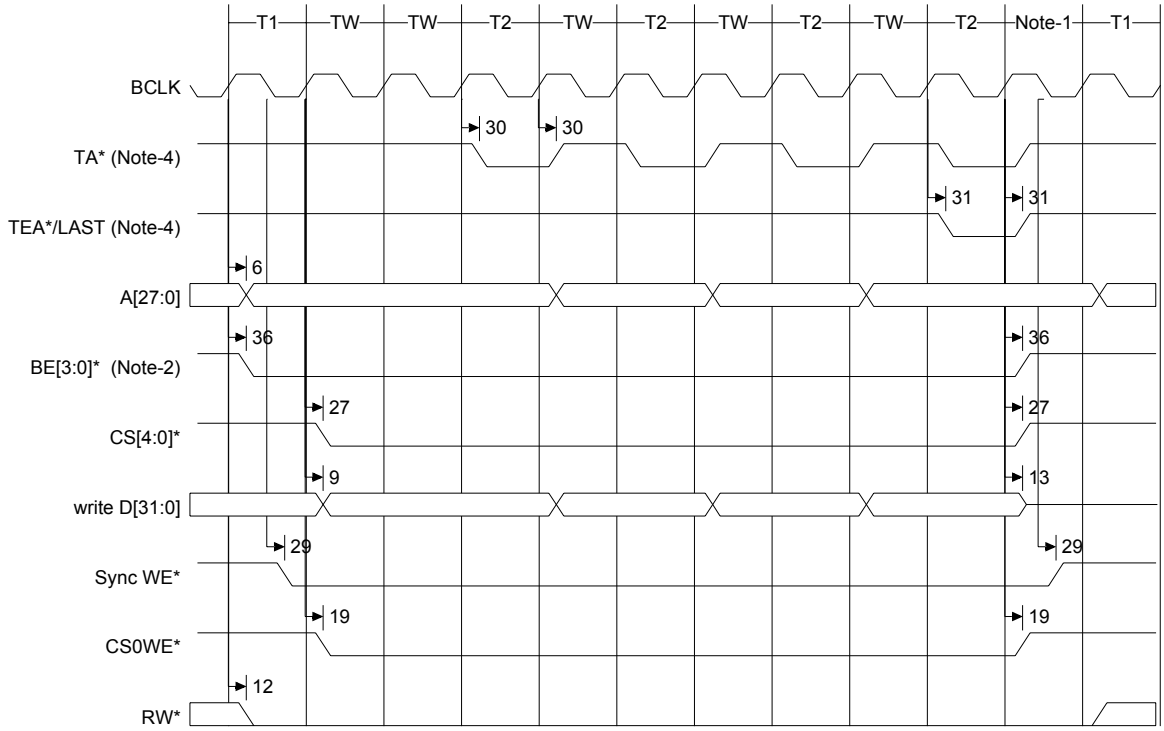
- 8-bit port = BE3*
- 16-bit port = BE[3:0]
- 32-bit port = BE[3:0]

3 The TW cycles are present when the WAIT field is set to 2 or more.

4 The TA* and TEA*/LAST signals are for reference only.

SRAM burst write

CS controlled, four word (4-2-2-2), burst write (wait = 2, BCYC = 01)



Notes:

1 If the next transfer is DMA, null periods between memory transfers can occur. Thirteen clock pulses are required for DMA context switching.

2 Port size determines which byte enable signals are active:

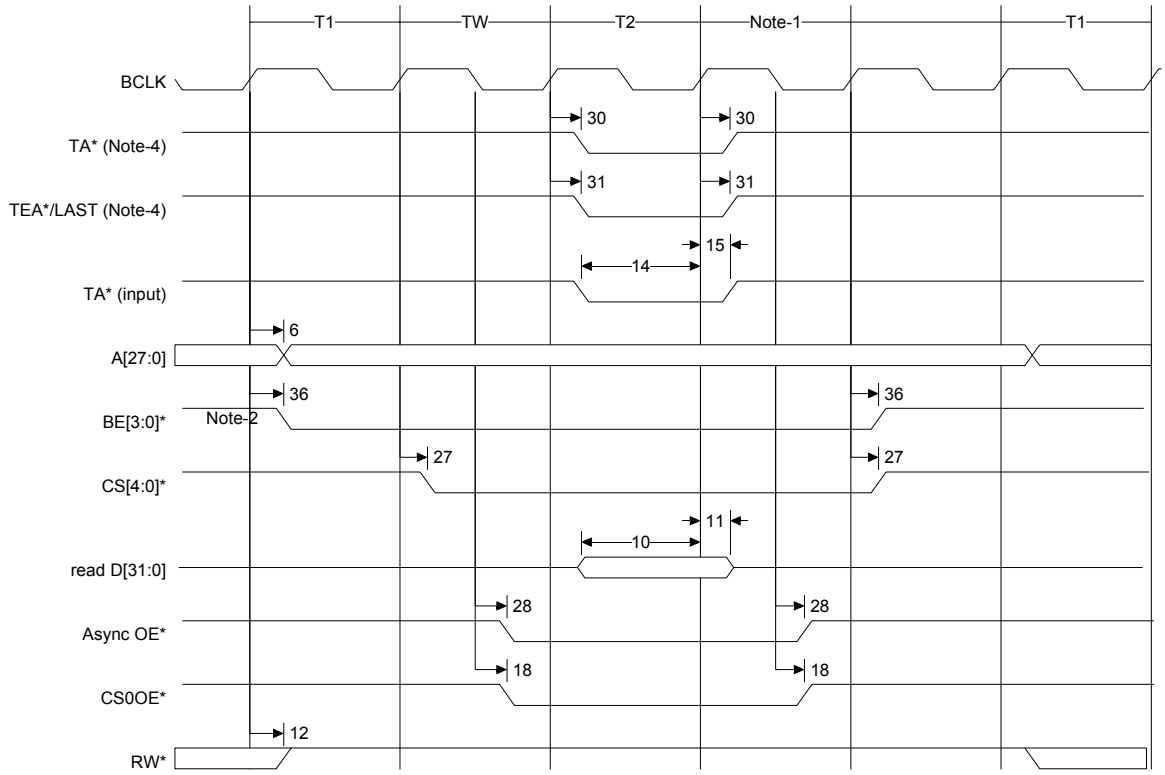
- 8-bit port = BE3*
- 16-bit port = BE[3:0]
- 32-bit port = BE[3:0]

3 The TW cycles are present when the WAIT field is set to 2 or more.

4 The TA* and TEA*/LAST signals are for reference only.

SRAM OE read

OE* controlled read (wait = 2)



Notes:

1 At least one null period occurs between memory transfers. More null periods can occur if the next transfer is DMA. Thirteen clock pulses are required for DMA context switching.

2 Port size determines which byte enable signals are active:

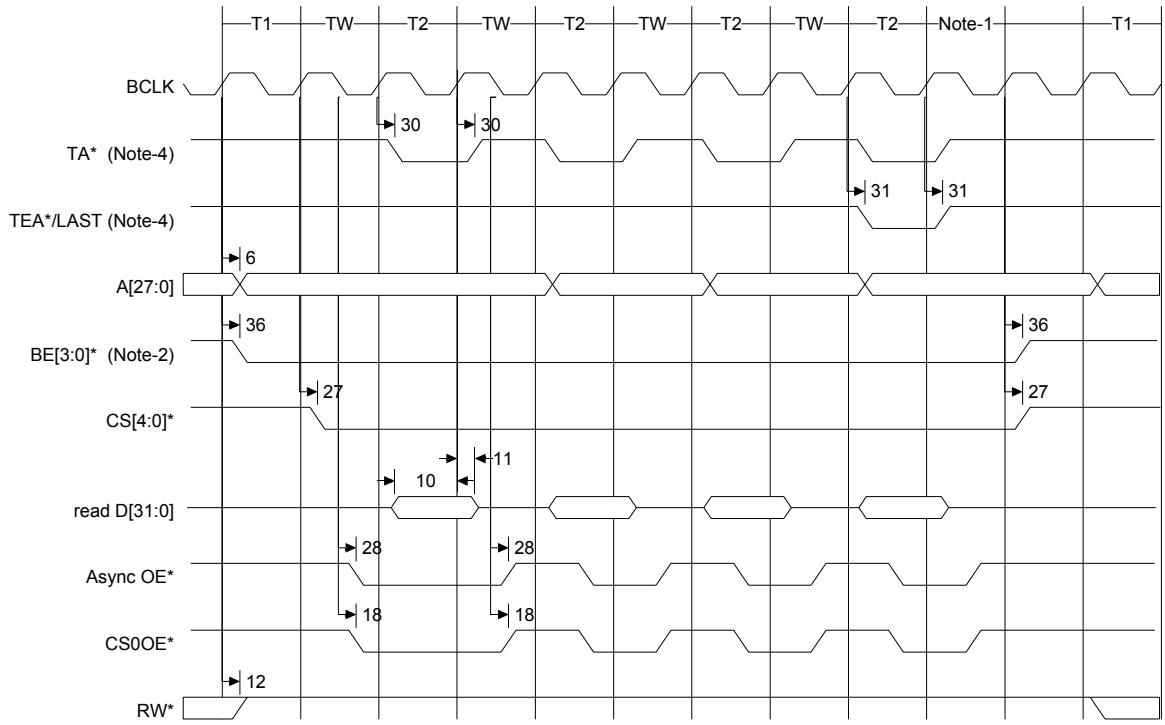
- 8-bit port = BE3*
- 16-bit port = BE[3:0]
- 32-bit port = BE[3:0]

3 The TW cycles are present when the WAIT field is set to 2 or more.

4 The TA* and TEA*/LAST signals are for reference only.

SRAM OE burst read

OE* controlled, four word (3-2-2-2), burst read (wait = 2, BCYC = 01)



Notes:

1 At least one null period occurs between memory transfers. More null periods can occur if the next transfer is DMA. Thirteen clock pulses are required for DMA context switching.

2 Port size determines which byte enable signals are active:

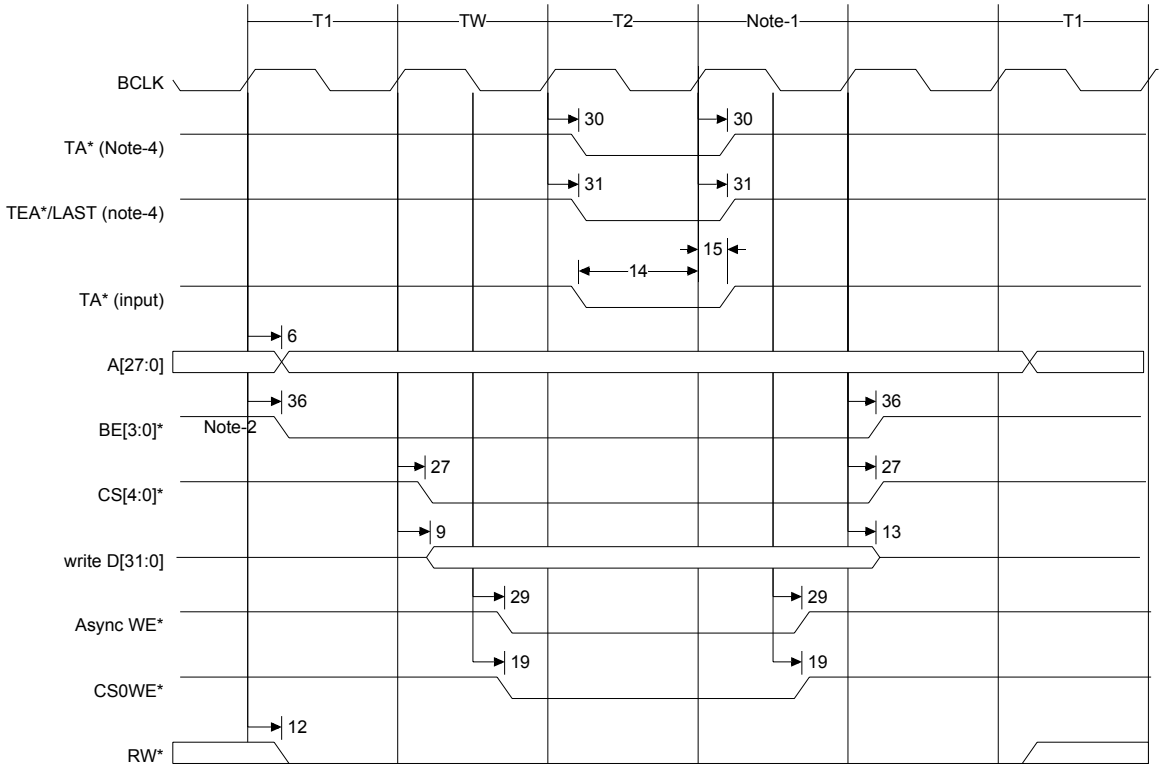
- 8-bit port = BE3*
- 16-bit port = BE[3:0]
- 32-bit port = BE[3:0]

3 The TW cycles are present when the WAIT field is set to 2 or more.

4 The TA* and TEA*/LAST signals are for reference only.

SRAM WE write

WE* controlled write (wait = 2)



Notes:

1 At least one null period occurs between memory transfers. More null periods can occur if the next transfer is DMA. Thirteen clock pulses are required for DMA context switching.

2 Port size determines which byte enable signals are active:

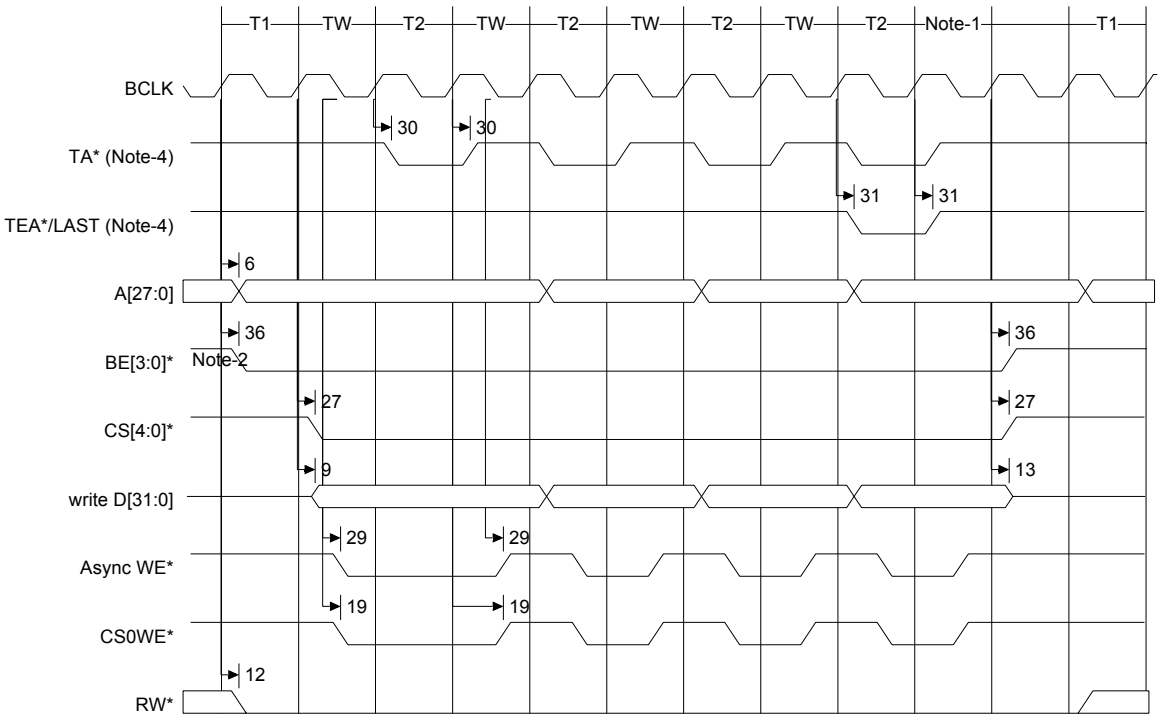
- 8-bit port = BE3*
- 16-bit port = BE[3:0]
- 32-bit port = BE[3:0]

3 The TW cycles are present when the WAIT field is set to 2 or more.

4 The TA* and TEA*/LAST signals are for reference only.

SRAM WE burst write

WE* controlled, four word (3-2-2-2), burst write (wait = 2, BCYC = 01)



Notes:

1 At least one null period occurs between memory transfers. More null periods can occur if the next transfer is DMA. Thirteen clock pulses are required for DMA context switching.

2 Port size determines which byte enable signals are active:

- 8-bit port = BE3*
- 16-bit port = BE[3:0]
- 32-bit port = BE[3:0]

3 The TW cycles are present when the WAIT field is set to 2 or more.

4 The TA* and TEA*/LAST signals are for reference only.

SDRAM timing

BCLK max frequency: 55.296 MHz

Operating conditions:

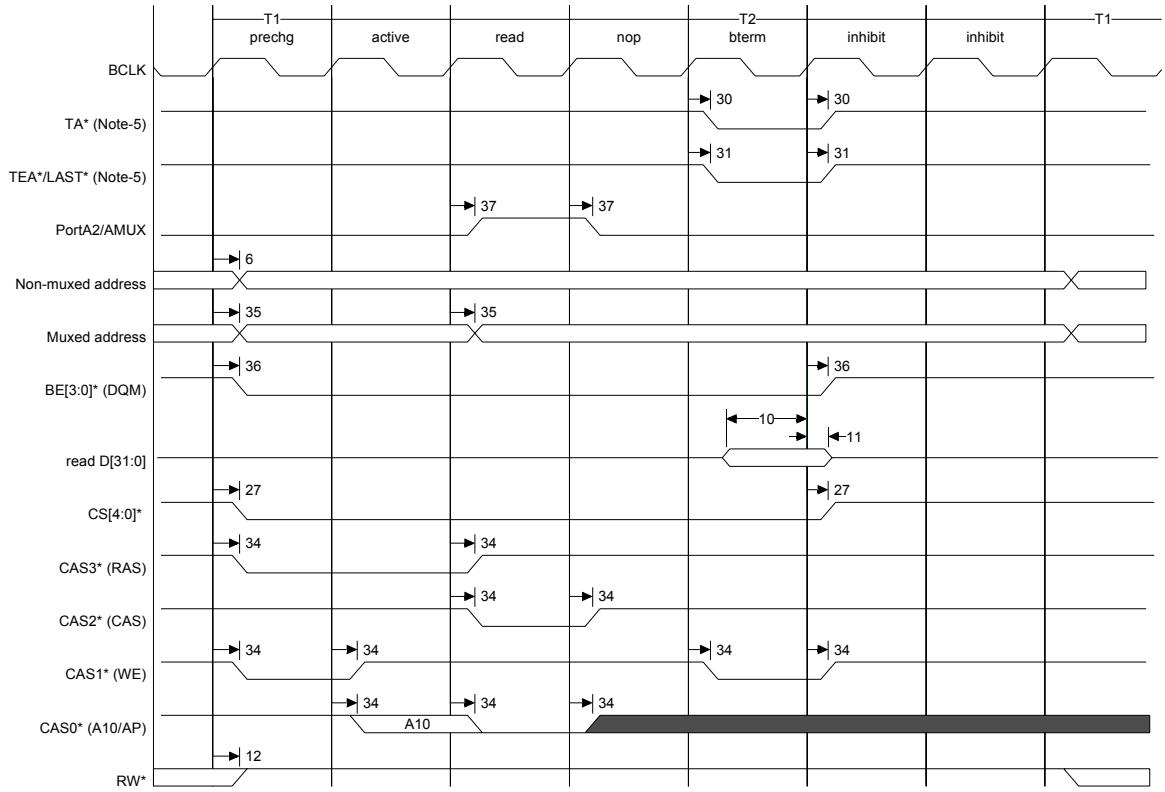
Temperature:	-15.00 (min)	110.00 (max)
Voltage:	1.60 (min)	1.40 (max)
Output load:	25.0pf	
Input drive:	CMOS buffer	

SDRAM timing parameters

Num	Description	Min	Max	Unit
36	BCLK high to BE*/DQM* valid		15.5	ns
6	BCLK high to non-muxed address valid	5	13.5	ns
9	BCLK high to data out valid		14	ns
13	BCLK high to data out high impedance		13	ns
10	Data in valid to BCLK high (setup)	5		ns
11	BCLK high to data in invalid (hold)	3		ns
27	BCLK high to CS* valid		15.5	ns
30	BCLK high to TA* valid		13.5	ns
31	BCLK high to TEA* valid		16	ns
37	BCLK high to PORTA2/AMUX valid		14	ns
35	BCLK high to muxed address valid	6	14.5	ns
34	BCLK high to CAS* valid		12	ns
12	BCLK high to RW* valid		13.5	ns

SDRAM read

SDRAM read, CAS latency = 2



Notes:

1 Port size determines which byte enable signals are active:
- 8-bit port = BE3*
- 16-bit port = BE[3:2]
- 32-bit port = BE[3:0]

2 The precharge and/or active commands are not always present. These commands depend on the address of the previous SDRAM access.

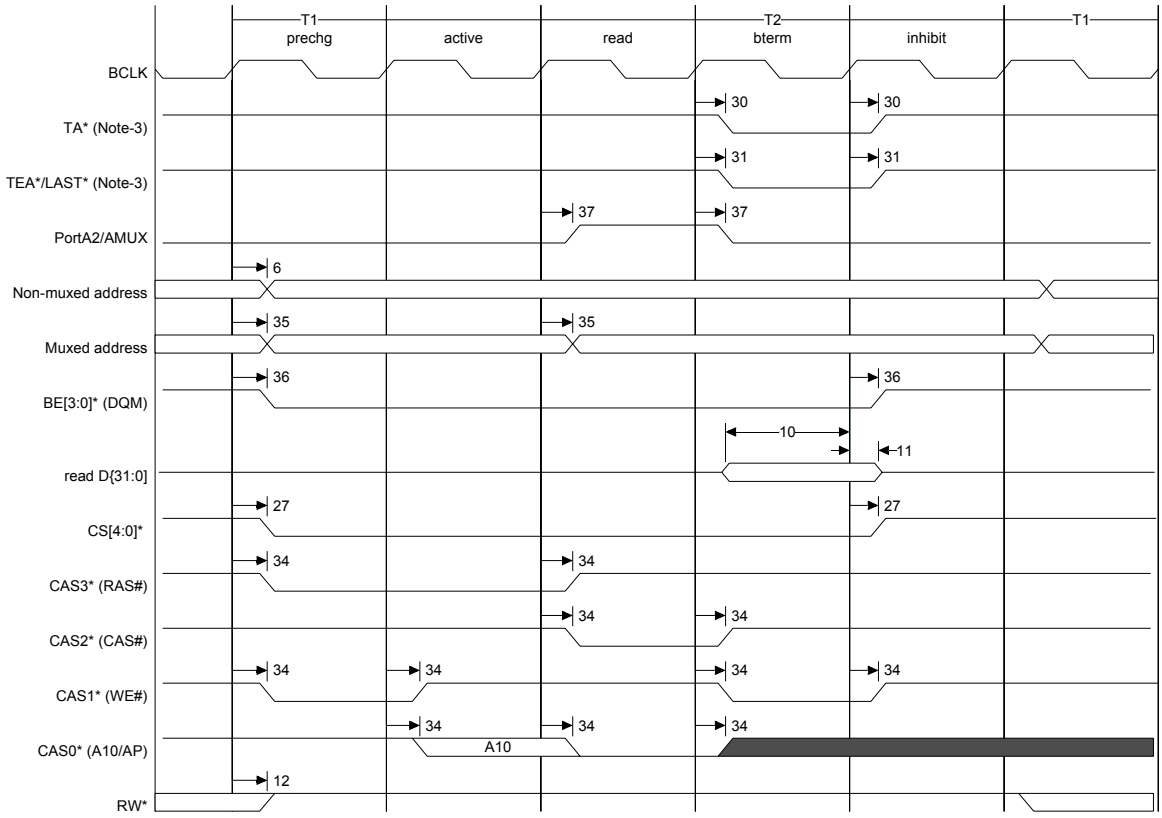
3 If CAS latency = 3, 2 NOPs occur between the read and burst terminate commands.

4 If CAS latency = 3, 3 inhibits occur after burst terminate.

5 The TA* and TEA*/LAST signals are for reference only.

SDRAM read

SDRAM read, CAS latency = 1



Notes:

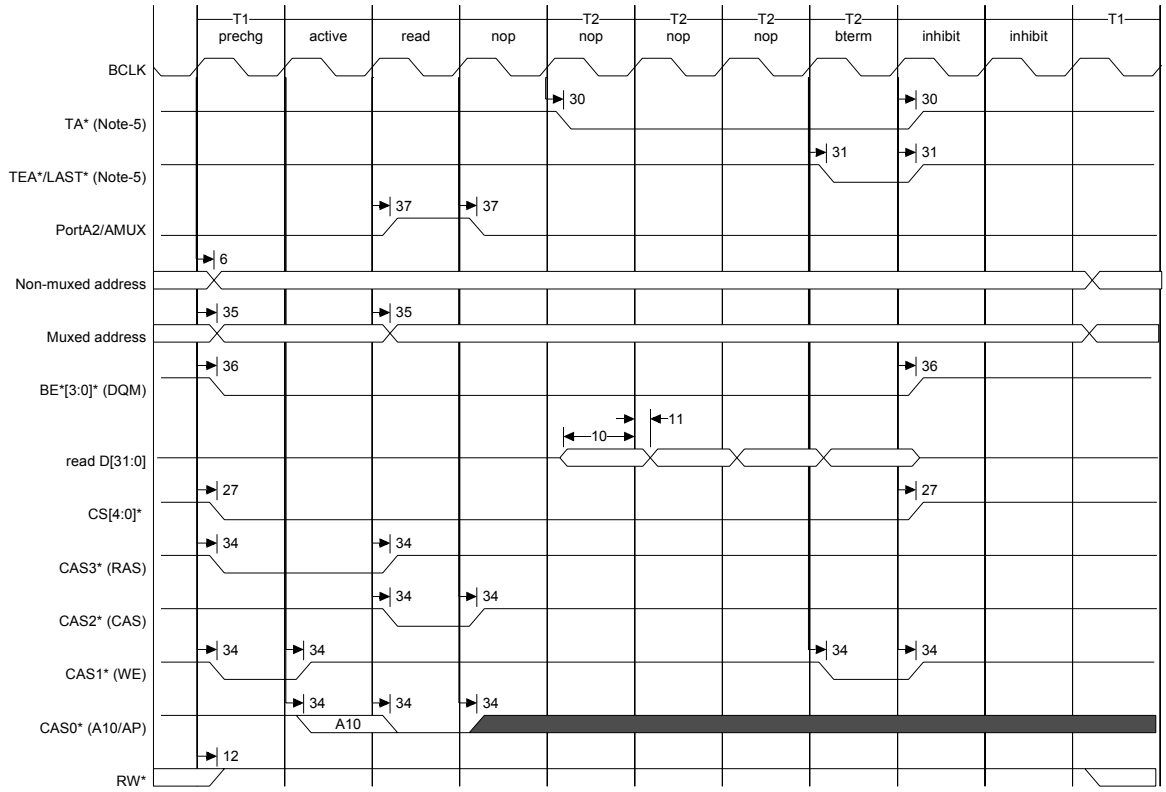
1 Port size determines which byte enable signals are active:
   - 8-bit port = BE3*
   - 16-bit port = BE[3:2]
   - 32-bit port = BE[3:0]

2 The precharge and/or active commands are not always present. These commands depend on the address of the previous SDRAM access.

3 The TA* and TEA*/LAST signals are for reference only.

SDRAM burst read

SDRAM read, CAS latency = 2



Notes:

1 Port size determines which byte enable signals are active:
- 8-bit port = BE3*
- 16-bit port = BE[3:2]
- 32-bit port = BE[3:0]

2 The precharge and/or active commands are not always present. These commands depend on the address of the previous SDRAM access.

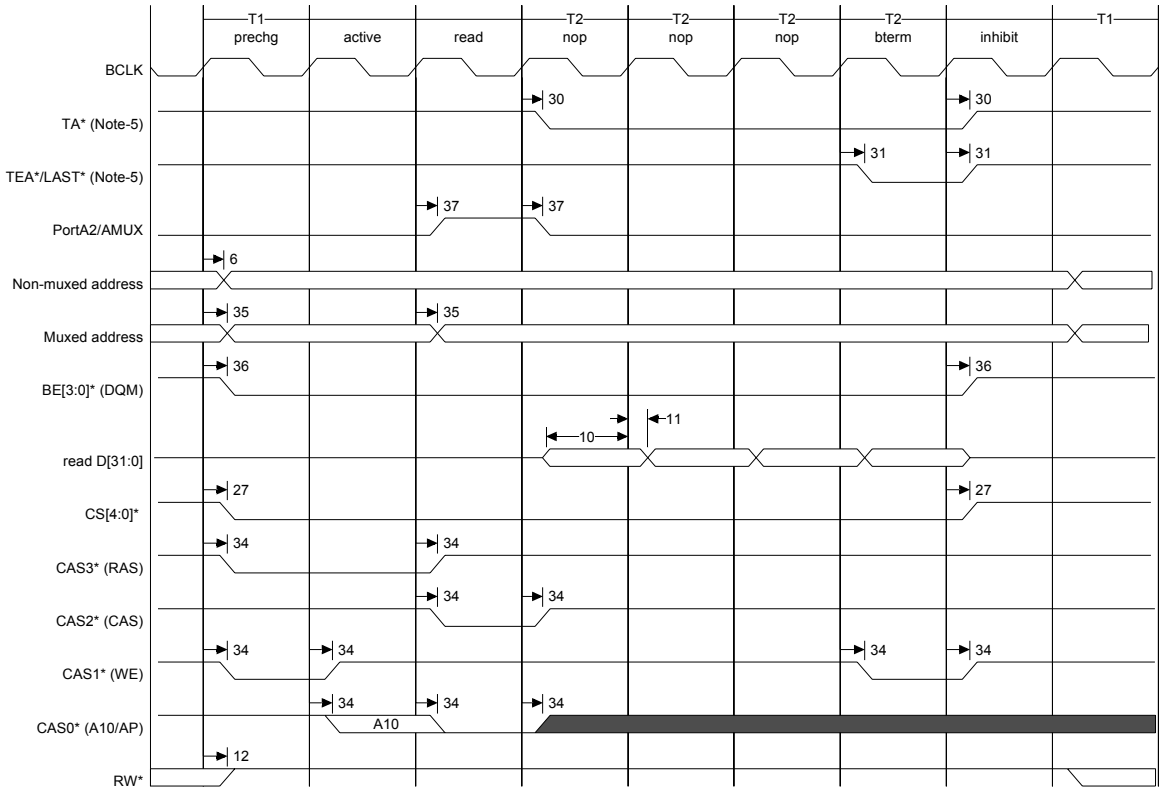
3 If CAS latency = 3, 5 NOPs occur between the read and burst terminate commands.

4 If CAS latency = 3, 3 inhibits occur after burst terminate.

5 The TA* and TEA*/LAST signals are for reference only.

SDRAM burst read

SDRAM read, CAS latency = 1



Notes:

1 Port size determines which byte enable signals are active:
- 8-bit port = BE3*
- 16-bit port = BE[3:2]
- 32-bit port = BE[3:0]

2 The precharge and/or active commands are not always present. These commands depend on the address of the previous SDRAM access.

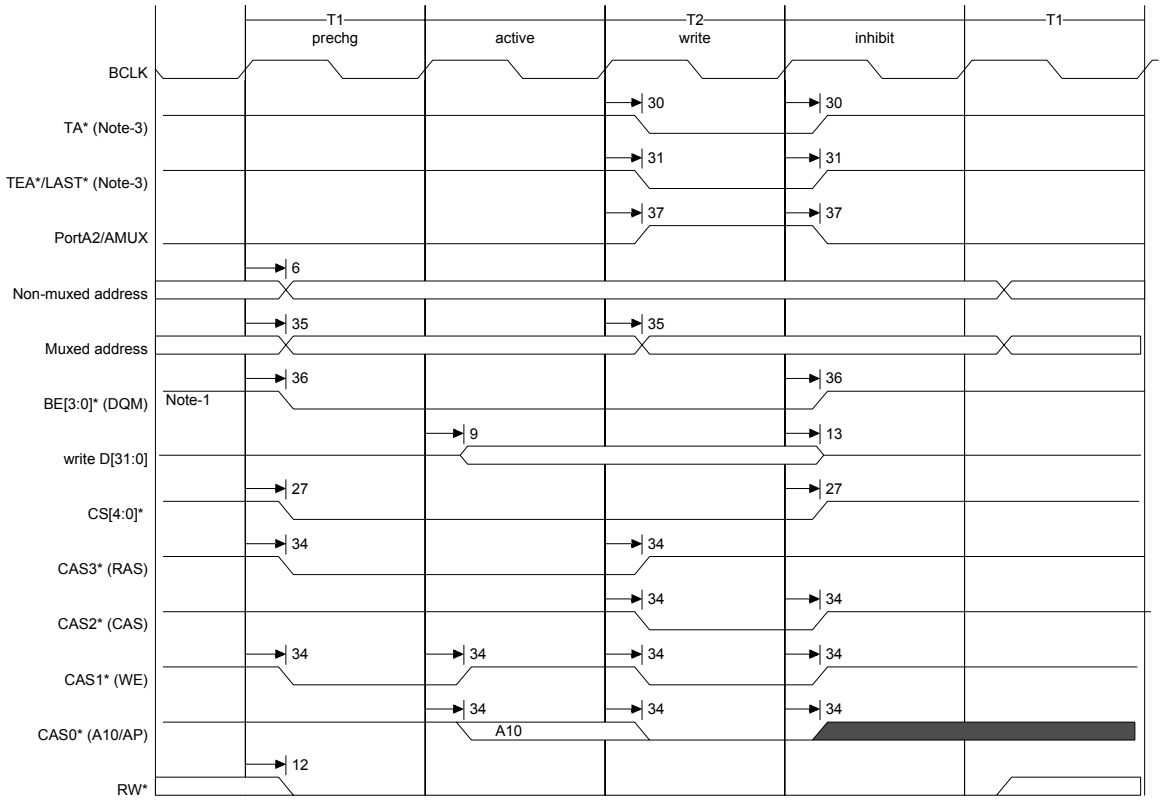
3 If CAS latency = 3, 5 NOPs occur between the read and burst terminate commands.

4 If CAS latency = 3, 3 inhibits occur after burst terminate.

5 The TA* and TEA*/LAST signals are for reference only.

SDRAM write

SDRAM write



Notes:

1 Port size determines which byte enable signals are active:

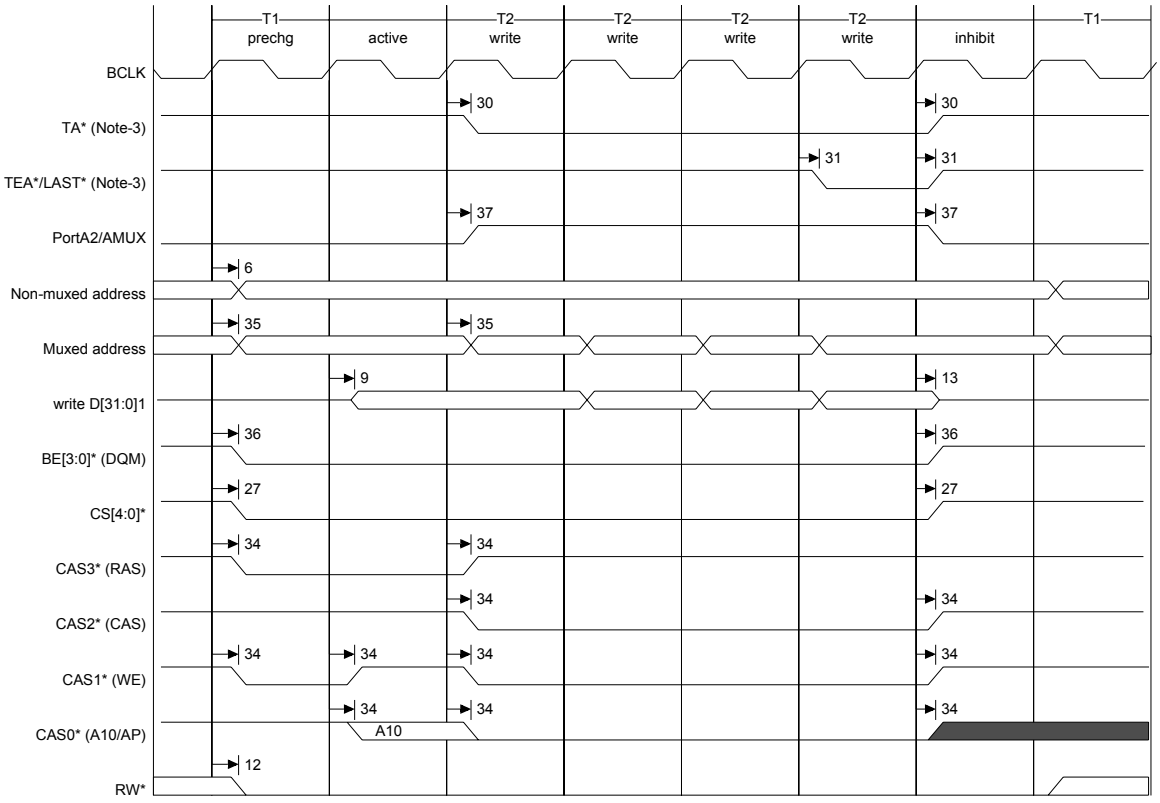
- 8-bit port = BE3*
- 16-bit port = BE[3:2]
- 32-bit port = BE[3:0]

2 The precharge and/or active commands are not always present. These commands depend on the address of the previous SDRAM access.

3 The TA* and TEA*/LAST signals are for reference only.

SDRAM burst write

SDRAM burst write



Notes:

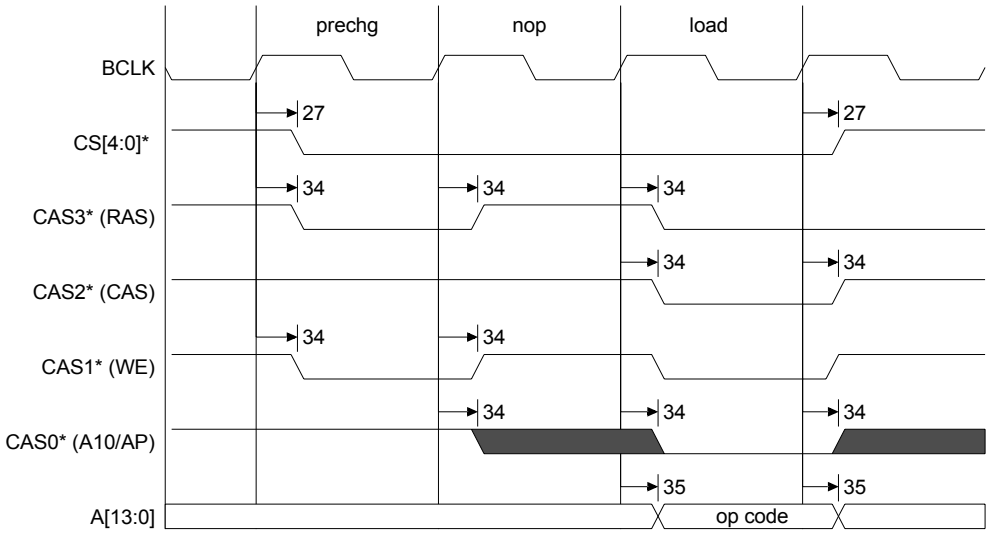
1 Port size determines which byte enable signals are active:

- 8-bit port = BE3*
- 16-bit port = BE[3:2]
- 32-bit port = BE[3:0]

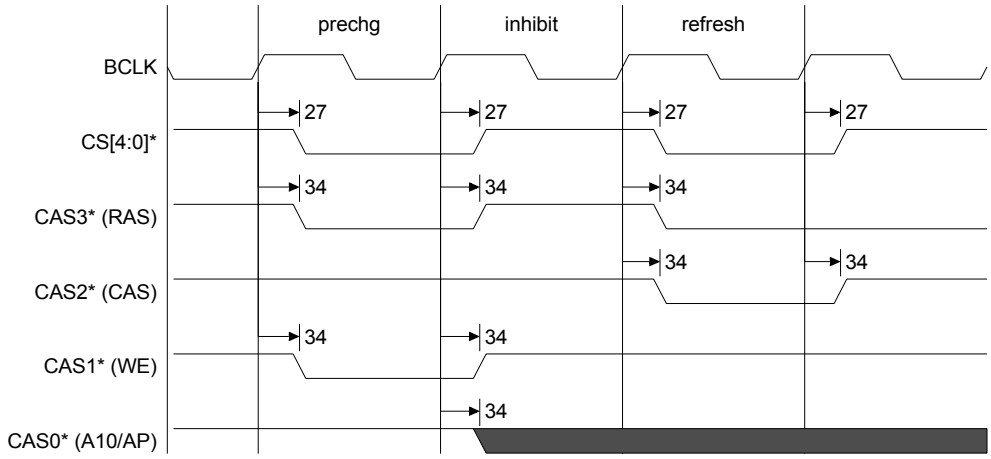
2 The precharge and/or active commands are not always present. These commands depend on the address of the previous SDRAM access. When the active command is not present, parameter #35 is valid during the write (T2) cycle.

3 The TA* and TEA*/LAST signals are for reference only.

SDRAM load mode



SDRAM refresh



FP DRAM timing

BCLK max frequency: 55.296 MHz

Operating conditions:

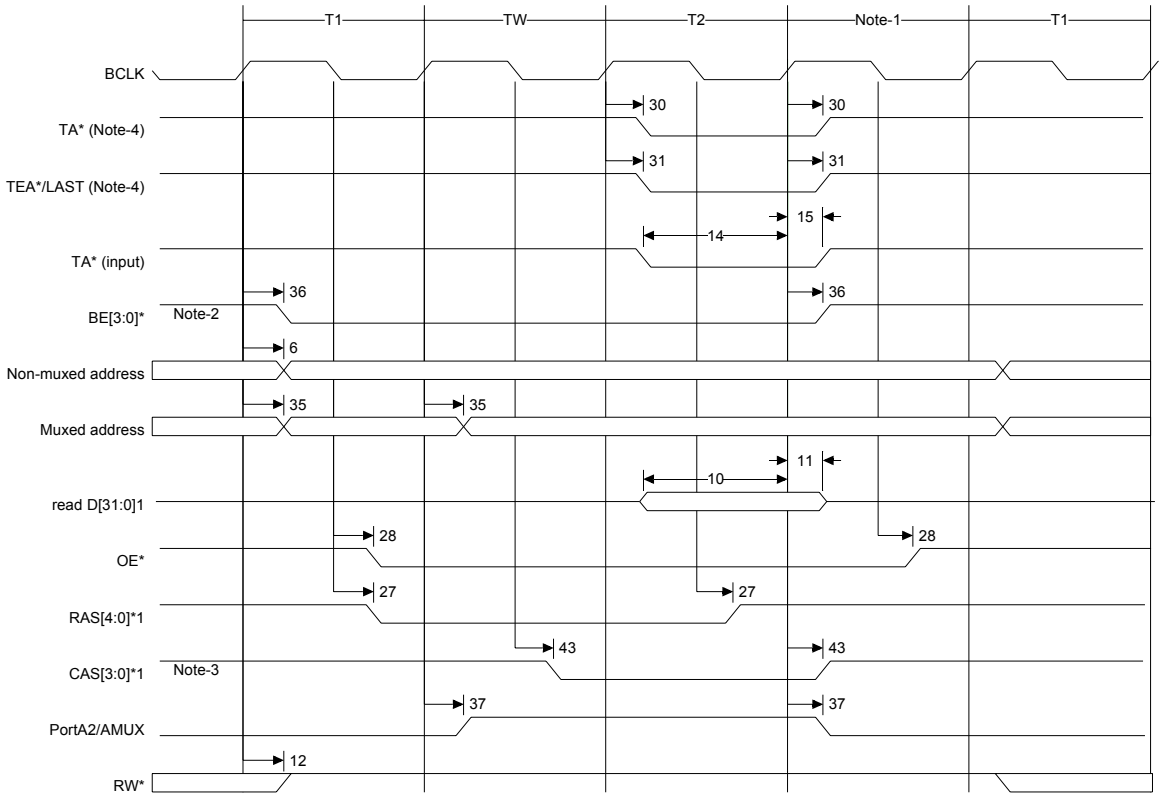
Temperature:	-15.00 (min)	110.00 (max)
Voltage:	1.60 (min)	1.40 (max)
Output load:	25.0pf	
Input drive:	CMOS buffer	

FP DRAM timing parameters

Num	Description	Min	Max	Unit
36	BCLK high to BE* valid		15.5	ns
6	BCLK high to address valid	5	13.5	ns
9	BCLK high to data out valid		14	ns
13	BCLK high to data out high impedance		13	ns
10	Data in valid to BCLK high (setup)	5		ns
11	BCLK high to data in invalid (hold)	3		ns
14	TA* valid to BCLK high (setup)	5		ns
15	BCLK high to TA* invalid (hold)	3		ns
28	BCLK low to OE* valid		12.5	ns
29	BCLK low to WE* valid		13	ns
30	BCLK high to TA* valid		13.5	ns
31	BCLK high to TEA* valid		16	ns
37	BCLK high to PORTA2/AMUX valid		14	ns
35	BCLK high to muxed address valid	6	14.5	ns
43	BCLK low to CAS* valid		13	ns
27	BCLK low to RAS* valid		12	ns
12	BCLK high to RW* valid		13.5	ns

FP DRAM read

Fast Page read



Notes:

1 If the next transfer is DMA, null periods between memory transfers can occur. Thirteen clock pulses are required for DMA context switching.

2 Port size determines which byte enable signals are active:

- 8-bit port = BE3*
- 16-bit port = BE[3:2]
- 32-bit port = BE[3:0]

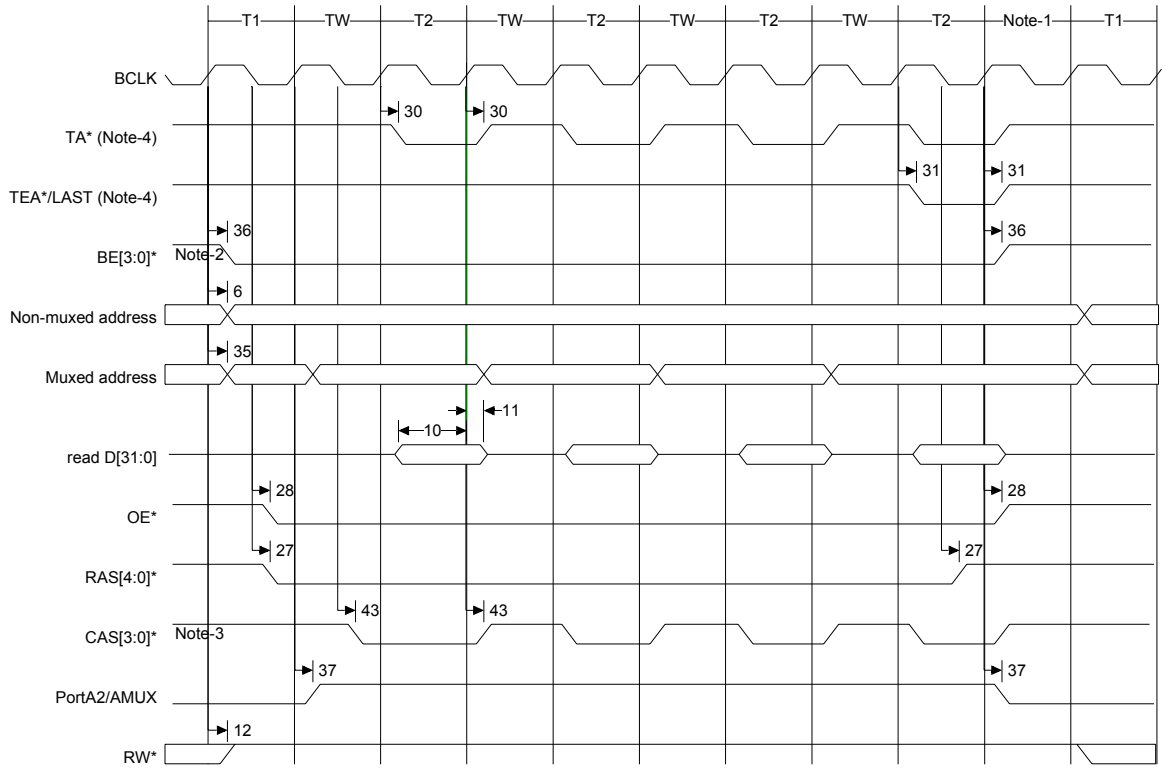
3 Port size determines which CAS signals are active:

- 8-bit port = CAS3*
- 16-bit port = CAS[3:2]
- 32-bit port = CAS[3:0]

4 The TA* and TEA*/LAST signals are for reference only.

FP DRAM burst read

Fast Page burst read



Notes:

1 If the next transfer is DMA, null periods between memory transfers can occur. Thirteen clock pulses are required for DMA context switching.

2 Port size determines which byte enable signals are active:

- 8-bit port = BE3*
- 16-bit port = BE[3:2]
- 32-bit port = BE[3:0]

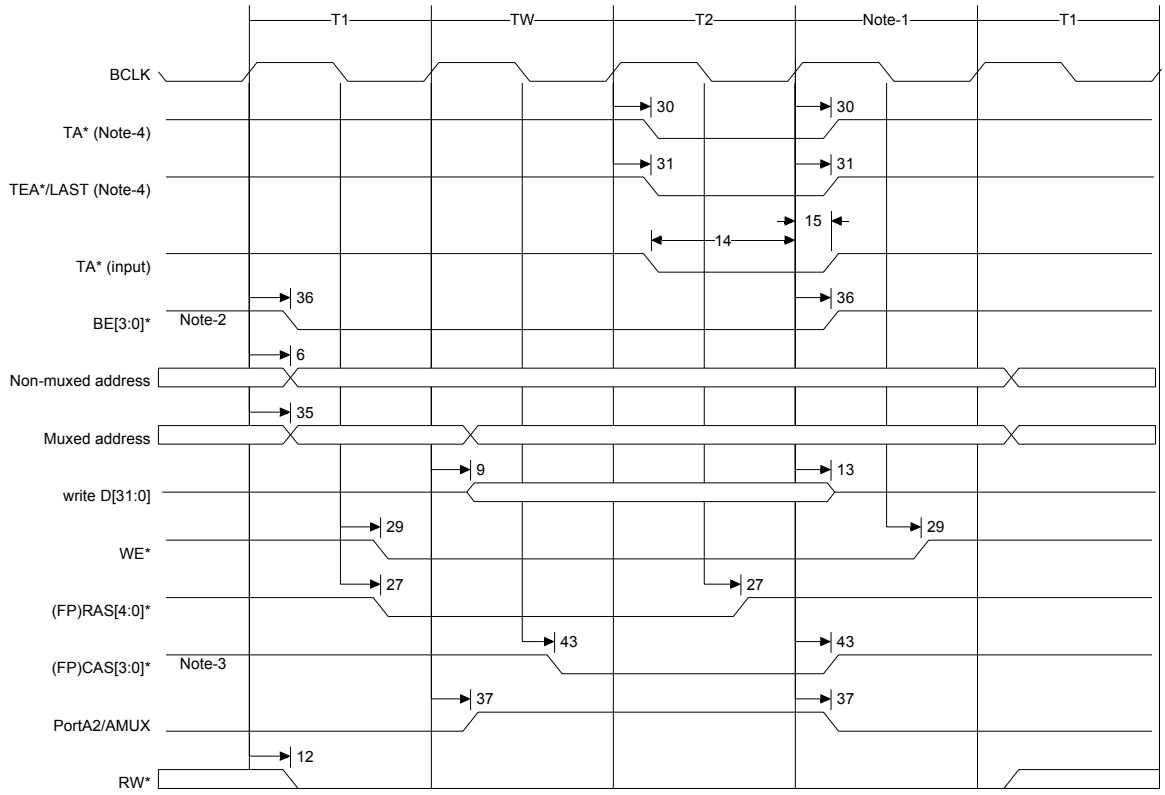
3 Port size determines which CAS signals are active:

- 8-bit port = CAS3*
- 16-bit port = CAS[3:2]
- 32-bit port = CAS[3:0]

4 The TA* and TEA*/LAST signals are for reference only.

FP DRAM write

Fast Page write



Notes:

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- 8-bit port = BE3*
- 16-bit port = BE[3:2]
- 32-bit port = BE[3:0]

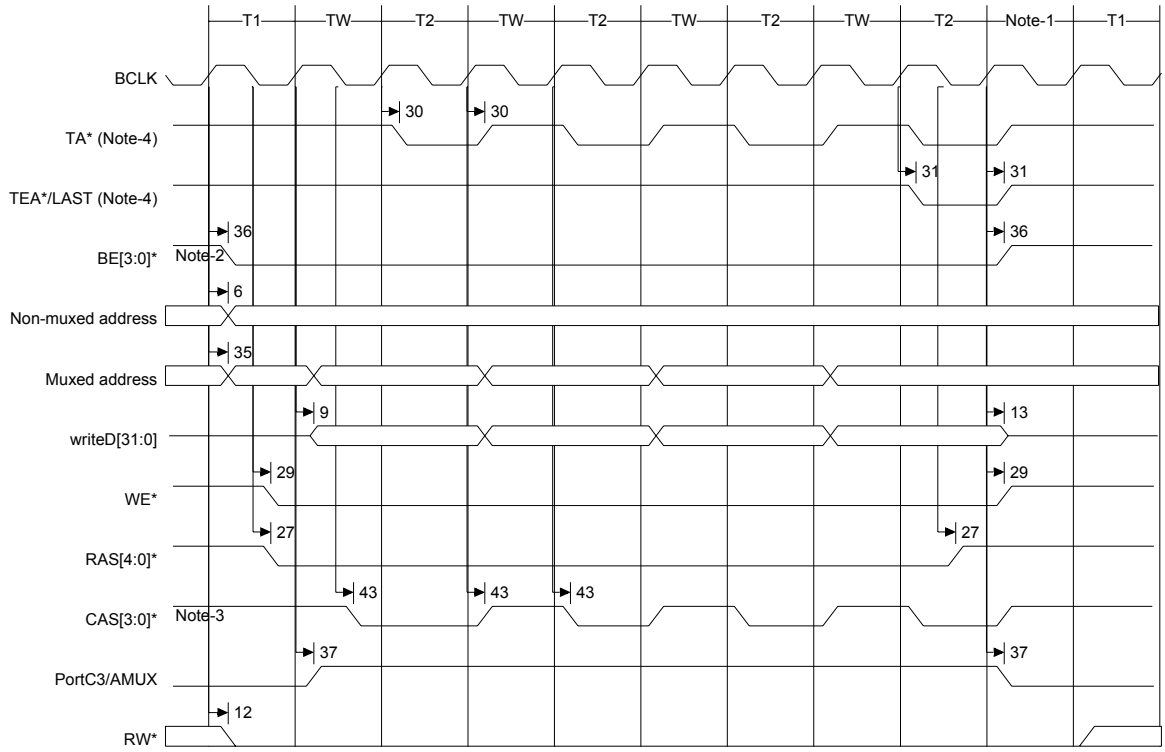
3 Port size determines which CAS signals are active:

- 8-bit port = CAS3*
- 16-bit port = CAS[3:2]
- 32-bit port = CAS[3:0]

4 The TA* and TEA*/LAST signals are for reference only.

FP DRAM burst write

Fast Page burst write



Notes:

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2 Port size determines which byte enable signals are active:

- 8-bit port = BE3*
- 16-bit port = BE[3:2]
- 32-bit port = BE[3:0]

3 Port size determines which CAS signals are active:

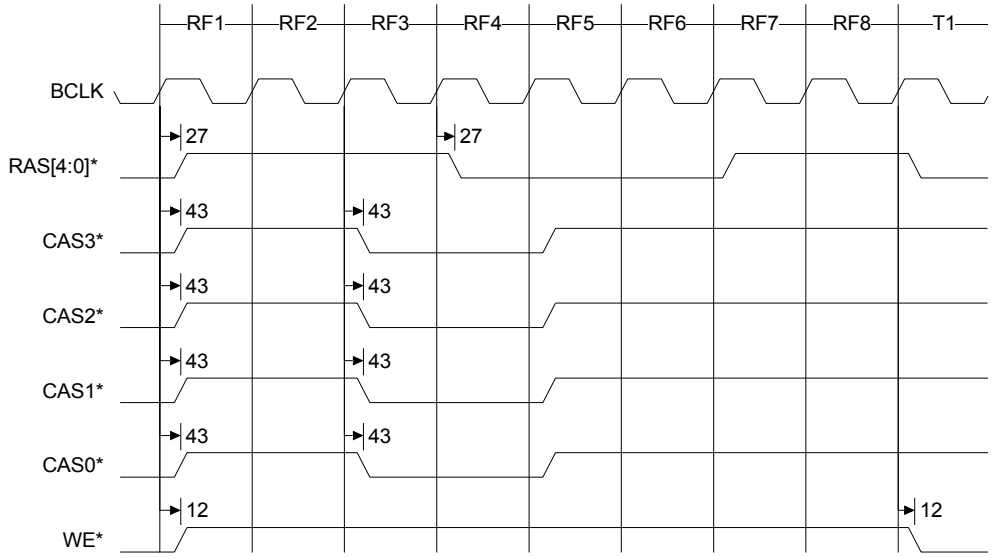
- 8-bit port = CAS3*
- 16-bit port = CAS[3:2]
- 32-bit port = CAS[3:0]

4 The TA* and TEA*/LAST signals are for reference only.

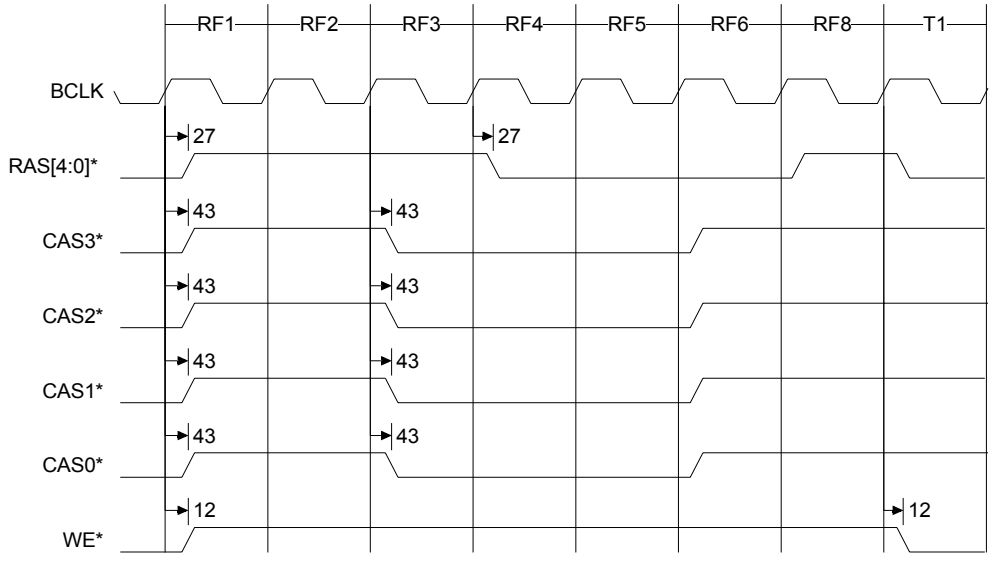
5 The BCYC field should never be set to 00.

fp_refresh_cycles

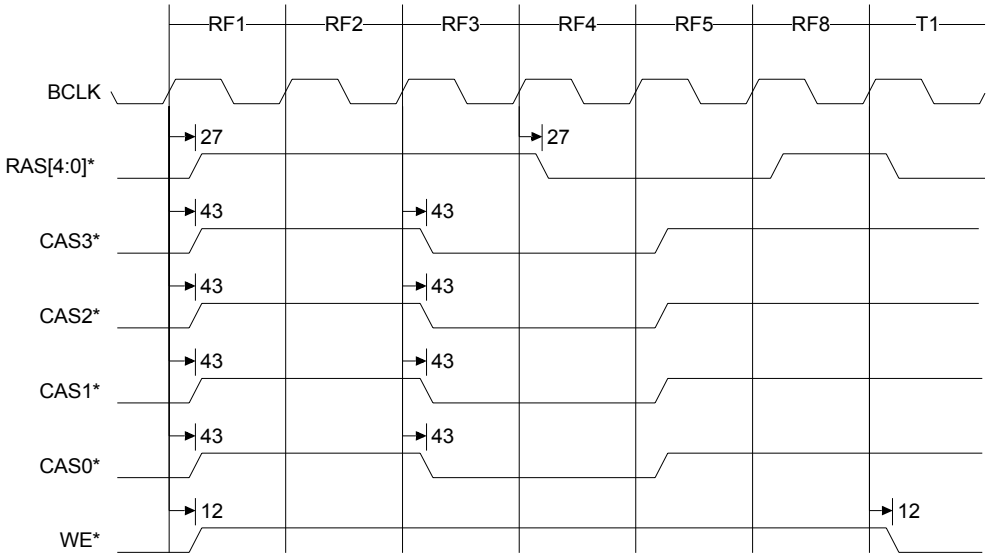
Fast page refresh (RCYC = 00)



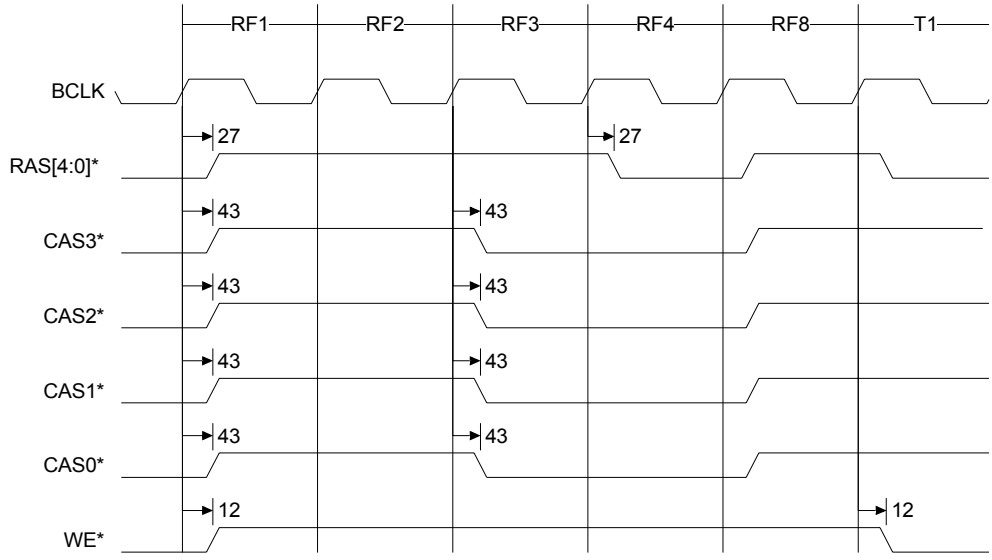
Fast page refresh (RCYC = 01)



Fast page refresh (RCYC = 10)



Fast page refresh (RCYC = 11)



Ethernet timing

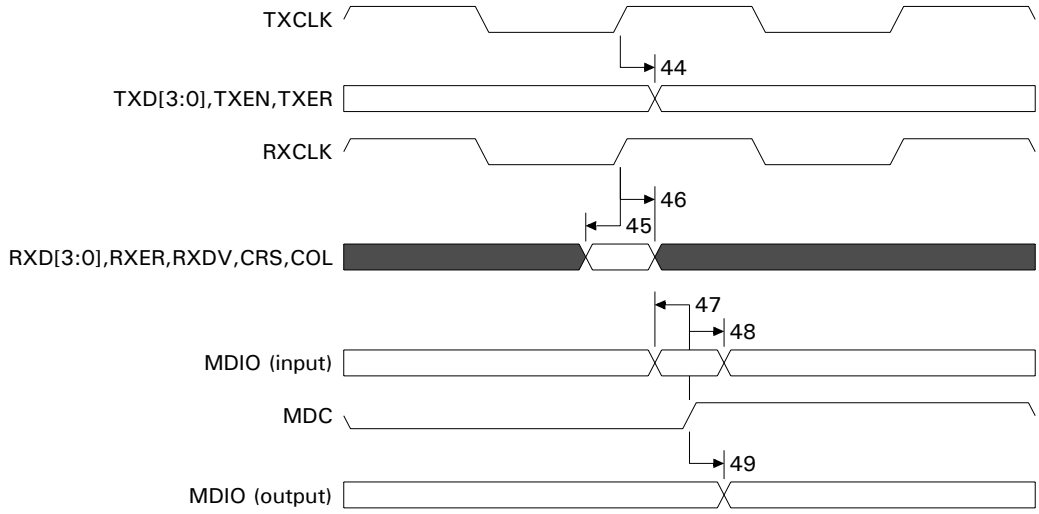
Operating conditions:

Temperature:	-15.00 (min)	110.00 (max)
Voltage:	1.60 (min)	1.40 (max)
Output load:	25.0pf	
Input drive:	CMOS buffer	

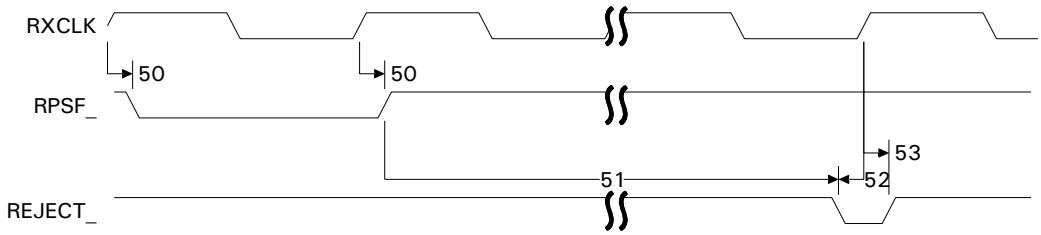
Ethernet timing parameters

Num	Description	Min	Max	Unit
44	TXCLK high to TXD*, TXEN, TXER valid		11.5	ns
45	RXD*, RXER, RXDV, TXCOL, RXCRS valid to RXCLK high (setup)	3		ns
46	RXCLK high to RXD*, RXER, RXDV, TXCOL, RXCRS hold time	2		ns
49	MDC high to MDIO valid		50	ns
47	MDIO valid to MDC high (setup)	3		ns
48	MDC high to MDIO hold time	3		ns
50	RXCLK high to RSPF* valid		15.5	ns
52	REJECT* valid to RXCLK high (setup)	3		ns
53	REJECT* valid from RXCLK high (hold)	1.5		ns

Ethernet PHY timing



Ethernet cam timing



JTAG timing

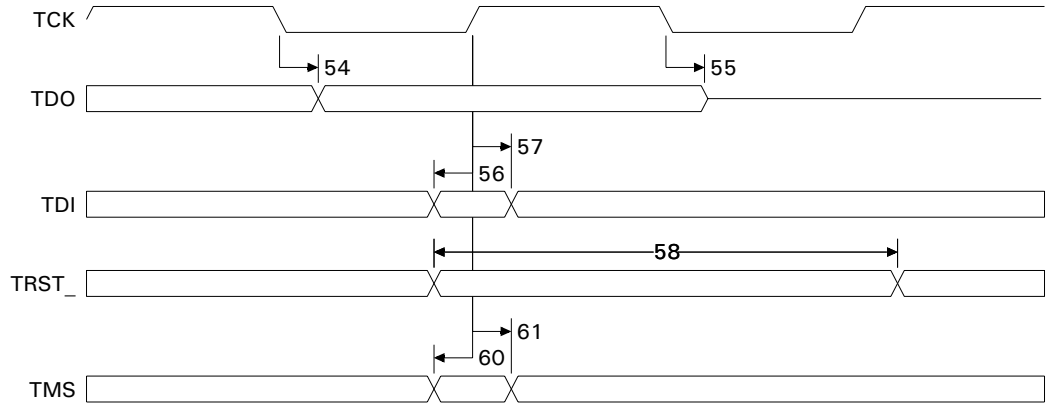
Operating conditions:

Temperature:	-15.00 (min)	110.00 (max)
Voltage:	1.60 (min)	1.40 (max)
Output load:	25.0pf	
Input drive:	CMOS buffer	

jtag arm ice timing parameters

Num	Description	Min	Max	Units
54	TCK to TDO valid		21	ns
55	TCK to TDO HighZ		21	ns
56	TDI setup to TCK rising	1		ns
57	TDI hold from TCK rising	3		ns
58	TRST* width	1		T_{TCK}
60	TMS setup to TCK rising	1		ns
61	TMS hold from TCK rising	3		ns

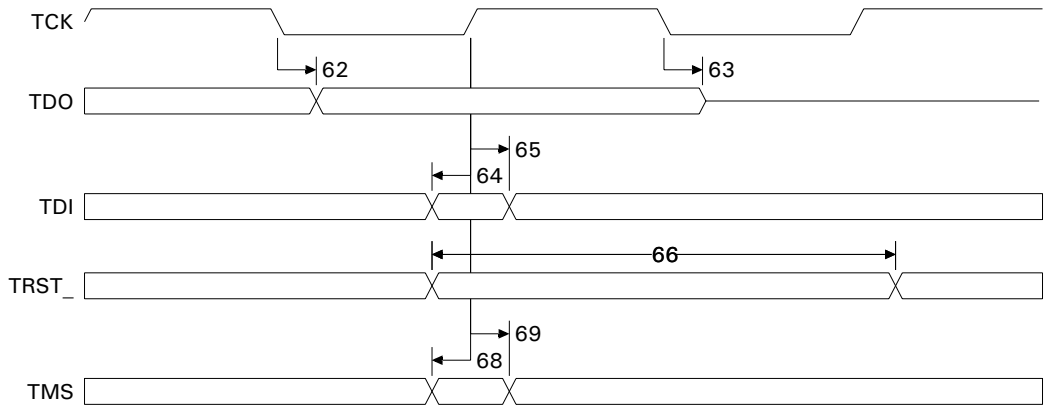
jtag arm ice timing diagram



jtag bscan timing parameters

Num	Description	Min	Max	Units
62	TCK to TDO valid		21	ns
63	TCK to TDO HighZ		21	ns
64	TDI setup to TCK rising	1		ns
65	TDI hold from TCK rising	3		ns
66	TRST* width	1		T_{TCK}
68	TMS setup to TCK rising	1		ns
69	TMS hold to TCK rising	3		ns

jtag bscan timing diagram



External DMA timing

BCLK max frequency: 55.296 MHz

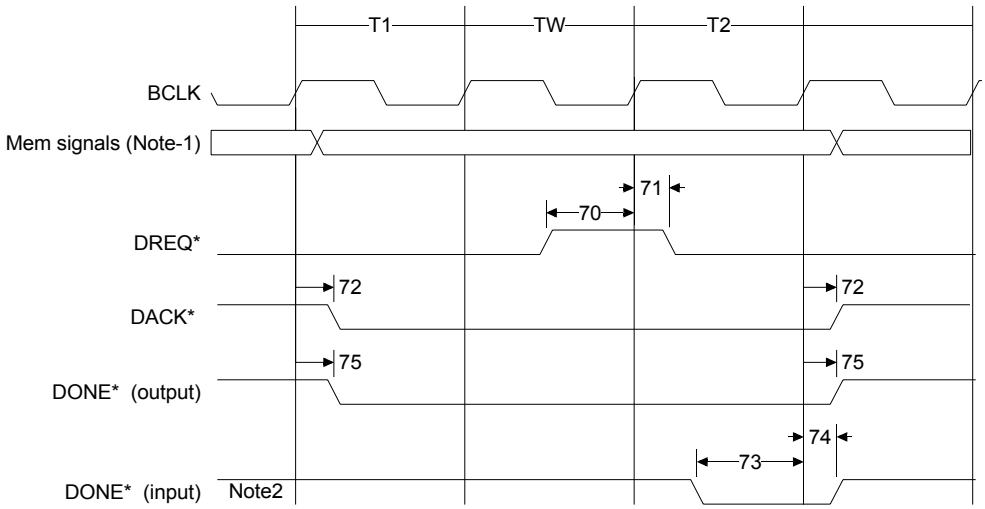
Operating conditions:

Temperature:	-15.00 (min)	110.00 (max)
Voltage:	1.60 (min)	1.40 (max)
Output load:	25.0pf	
Input drive:	CMOS buffer	

External DMA timing parameters

Num	Description	Min	Max	Unit
72	BCLK high to DACK* valid		14	ns
75	BCLK high to DONE* (output) valid		15	ns
70	DREQ* low to BCLK high (setup)	5		ns
71	BCLK high to DREQ* valid (hold)	0		ns
73	DONE* (input) valid BCLK high (setup)	5		ns
74	BLCK high to DONE* (input) valid (hold)	0		ns

Fly-by external DMA

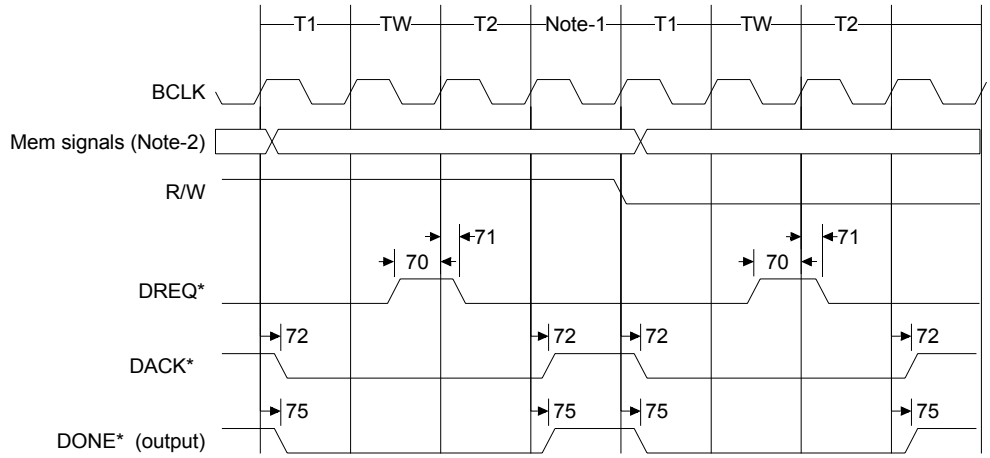


Notes:

1 The memory signals are data[31:0], addr[27:0], BE[3:0], CS/RAS[4:0], CAS[3:0], RW, OE*. WE*, and PORTC3/AMUX. The timing of these signals depends on how the memory is configured (Sync SRAM, Async SRAM, FP DRAM, or SDRAM).

2 The DONE* signal works as an input only when the DMA channel is configured as fly-by write.

Memory-to-memory external DMA



Notes:

1 A null period sometimes occurs between memory cycles.

1 The memory signals are data[31:0], addr[27:0], BE[3:0], CS/RAS[4:0], CAS[3:0], RW, OE*. WE*, and PORTA2/AMUX. The timing of these signals depends on how the memory is configured (Sync SRAM, Async SRAM, FP DRAM, or SDRAM).

Serial internal/external timing

Operating conditions:

Temperature:	-15.00 (min)	110.00 (max)
Voltage:	1.60 (min)	1.40 (max)
Output load:	25.0pf	
Input drive:	CMOS buffer	

Serial internal timing characteristics

Num	Description	Min	Max	Unit
76	SCLK to ENABLE high	1		T_{SCLK}
77	SCLK to TXD (PORTA7/C7)		1 T_{SYS}*	ns
78	RXD (PORTA3/C3) setup to SCLK	1		ns
79	RXD hold to SLK	1		ns

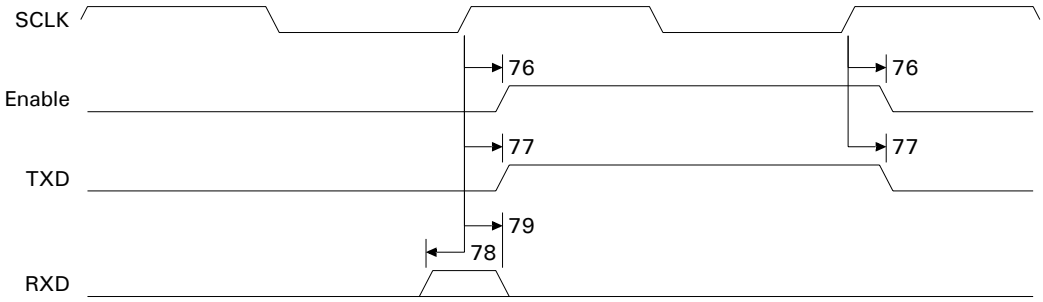
* The T_{SYS} parameter represents one period of the internal system clock.

Serial external timing characteristics

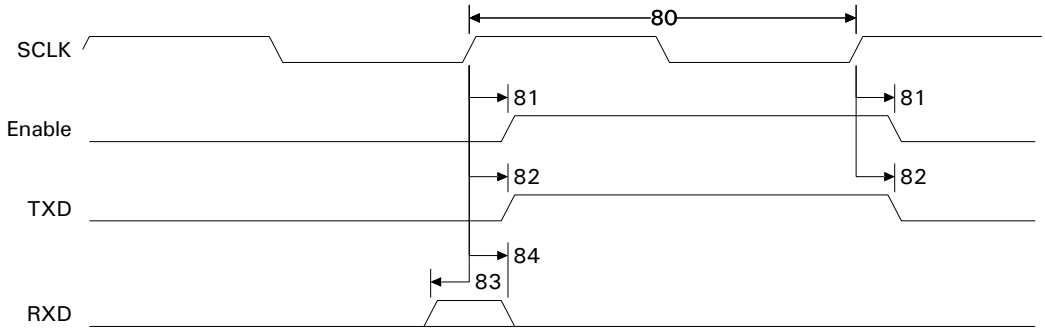
Num	Description	Min	Max	Unit
80	SCLK frequency		10	MHz
	SCLK duty cycle	45	55	%
81	SCLK to ENABLE	1		T_{SCLK}
82	SCLK to TXD (PORTA7/C7)		$2T_{SYS}$*	ns
83	RXD (PORTA3/C3) setup to SCLK	2		ns
84	RXD hold to SCLK	1.5		ns

* The T_{SYS} parameter represents one period of the internal system clock.

synchronous serial internal clock



synchronous serial external clock



GPIO timing

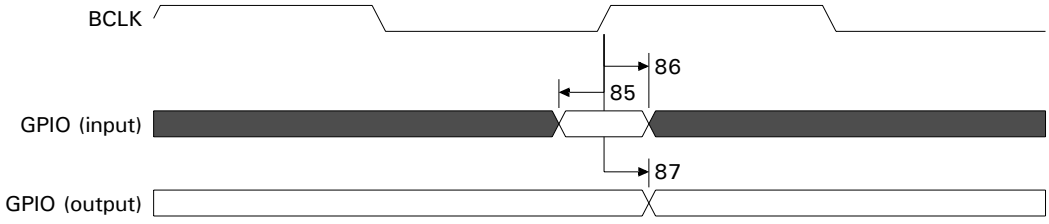
Operating conditions:

Temperature:	-15.00 (min)	110.00 (max)
Voltage:	1.60 (min)	1.40 (max)
Output load:	25.0pf	
Input drive:	CMOS buffer	

GPIO timing parameters

Num	Description	Min	Max	Unit
85	GPIO (setup) to BCLK rising	3		ns
86	GPIO (hold) from BCLK rising	0		ns
87	BCLK to GPIO (output)		17	ns

GPIO timing diagram



P/N: 90000303_C

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