UNCBASCF Base Board

User's Manual

PO Box 292528, 43229
☎+1 888 546 9741
info@es-usa.com

- Columbus OH (USA)
- Fax +1 888 546 9741
- www.es-usa.com

Kueferstrasse 8
☎+49 7667 908-0
sales@fsforth.de

- Breisach (Germany)
- Fax +49 7667 908-200
- www.fsforth.de

Calvo Sotelo 1, 1º - Dcha
☎+34 941 270 060
sitemas@embebidos.com

- Logroño (Spain)
- Fax +34 941 237 770
- www.embebidos.com

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Author: Héctor Palacios
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1. History

Date	Version	Responsible	Description
2003-11-06	0.3	Nigel James	Release
2003-10-20	0.2	Pedro Pérez de Heredia	Revision
2003-10-17	0.1	Héctor Palacios	Initial version

2. General

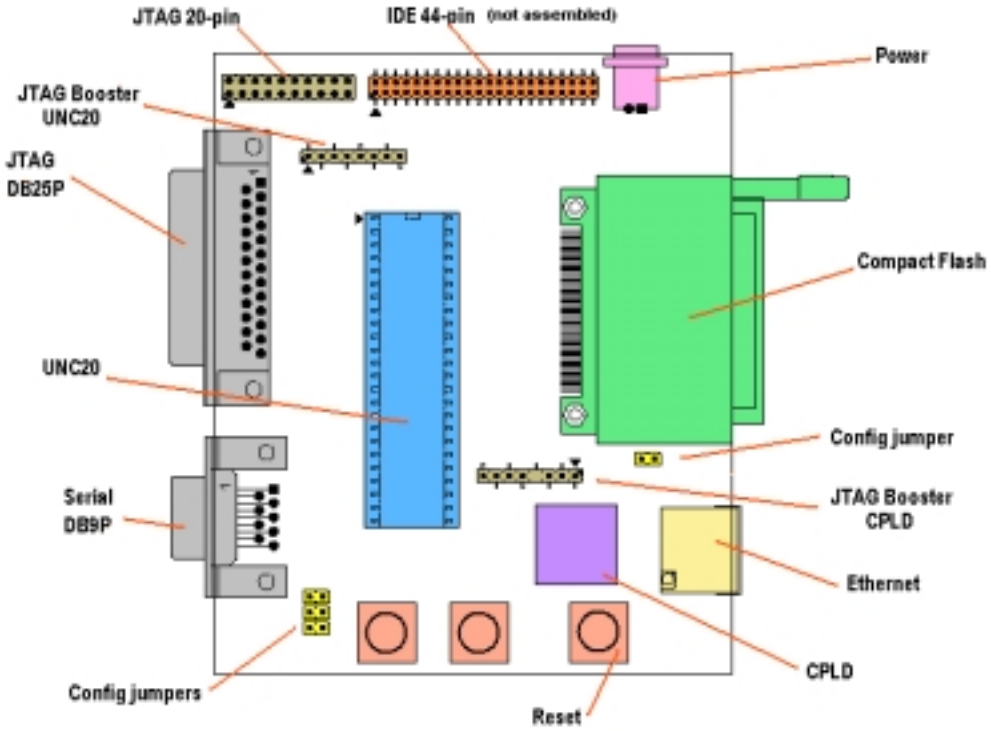
The UNCBASCF is a modified version of the standard UNC20 base board with support for CompactFlash cards.

This document refers to the UNCBASCF_0 revision of the board. The board's name is printed on the PCB and can also be found on the label, above the serial number.

3. Features

- Base board which accommodates one UNC20 module
- Ethernet interface with RJ45 connector with integrated link LED
- 1 serial communication RS232 interface
- JTAG interface
- LEDs for Power, Hard Disk and Ethernet Link
- 2 switches and 2 LEDs for use by application
- Reset switch
- CPLD programmed for CompactFlash interface
- CompactFlash connector (type 2)

4. Block Diagram of Base Board



5. Detailed Description

5.1. UNC20 Module

The UNC20 module is a cost-effective, highly integrated module in a 48-pin dual-inline package.

The salient features of the UNC20 module, as delivered with the Developer's Kit, are listed below:

- NetSilicon's NS7520 microcontroller based on a 32-bit ARM7TDMI core
- 16 Mbytes SDRAM
- 8 Mbytes Flash
- Ethernet interface
- 2 serial communication interfaces
- I2C interface
- JTAG interface

Please refer to the UNC20 User's Manual for more details on this module.

The pin-out for the UNC20 module can be found at the end of this manual.

5.2. RS232 Serial Interface

The NS7520 provides two serial ports. Since these ports are multiplexed with the General Purpose I/O pins (ports A and C), it was decided only to assemble one serial port and leave the other for the user to configure.

5.2.1. Serial Port 1

Serial Port 1 can be used as a console port to communicate with a host PC.

An RS232 driver, the MAX3320 from Maxim, is assembled on the base board. This driver guarantees baudrates up to 250kbps.

This port will operate in asynchronous RS232 full-duplex mode. The RS232 port supports minimal hardware control signals, namely RTS and CTS only, and is derived from the UNC20 module's Port C pins.

A 9-pin D-type connector (male) is assembled on the base board.

The pin allocation of the 9-pin D-type connector is as defined in the table below:

Pin	Function
1	N/C
2	RXD
3	TXD
4	N/C
5	GND
6	N/C
7	RTS
8	CTS
9	N/C

If a serial console is not required, and the 4 PortC pins are required for GPIO, then the serial driver can be forced into an “off” state, meaning that the on-chip power supply is shut down, by connecting a jumper between pins 3 and 4 of J1.

Pin	A	Description when inserted	Factory default
▌3		Serial driver forced off	Not inserted
▌4			

Jumper settings for J1 ▌= connected pins

To disable the serial driver, the jumper has to be inserted.

5.2.2. Serial Port 2

Serial Port 2 is available on the UNC20 module’s Port A [0-7] pins, which are led out to the X6 connector (not assembled on the board), so that users can configure this port to suit their application.

5.3. Ethernet

The 10/100 Ethernet MAC controller and PHY are included on the UNC20 module.

An RJ45 jack is used with a status LED for Link/Activity which is visible through a light pipe in the jack. A separate Pulse transformer is assembled.

The pin allocation of the RJ45 connector is as defined in the table below:

Pin	Function
1	TD+
2	TD-
3	RD+

4	N/C
5	N/C
6	RD-
7	N/C
8	N/C

5.4. CompactFlash

The UNCBASCF is equipped with a type 2 CompactFlash card holder.

The CompactFlash cards can be accessed using different hardware interface methods. Each one of these hardware interface methods has its own set of performance, cost and flexibility requirements. The choices are as follows:

- True IDE Mode
- Common Memory Mode
- I/O Mapped Mode

The True IDE mode can only be used with CompactFlash storage cards, while the other modes allow the use of any kind of CompactFlash card (wireless, network, storage,…).

A CPLD on the bottom side of the UNCBASCF base board has been programmed to implement PC card Common Memory and PC card I/O modes. The source code of the CPLD program is delivered with the UNC20 Developer's Kit with CompactFlash.

Although the hardware is prepared for all available modes (True IDE, Common Memory and I/O) the CPLD has been factory programmed to handle only the Common Memory mode and IO modes. **The CPLD of the UNCBASCF can be programmed for True IDE mode on demand**.

IMPORTANT NOTE: Jumper J4 is only used for True IDE mode. For normal use in Common Memory / IO modes, this jumper must be removed to avoid CPLD damage!

IMPORTANT NOTE: Jumper J1/1-2 is only required when programming the Flash on the UNC20. In normal operation it should not be present, otherwise it is not possible to access the CompactFlash cards.

IMPORTANT NOTE: Plug and play of CompactFlash cards is not supported! Never insert or remove your CompactFlash card while the target is powered on.

5.4.3. CompactFlash connector

The following table shows the functions of each pin of the CompactFlash connector, depending on the working mode:

Pin	TRUE IDE	MEMORY	I/O
1	GND	GND	GND
2	D19	D19	D19
3	D20	D20	D20
4	D21	D21	D21
5	D22	D22	D22
6	D23	D23	D23
7	CS0#	CE1#	CE1#
8	GND	A10	A10
9	ATA_SEL#	OE#	OE#
10	GND	A9	A9
11	GND	A8	A8

12	GND	A7	A7
13	VCC	VCC	VCC
14	GND	A6	A6
15	GND	A5	A5
16	GND	A4	A4
17	GND	A3	A3
18	A2	A2	A2
19	A1	A1	A1
20	A0	A0	A0
21	D16	D16	D16
22	D17	D17	D17
23	D18	D18	D18
24	IOCS16#	WP	IOIS16#
25	CD2#	CD2#	CD2#
26	CD1#	CD1#	CD1#
27	D27	D27	D27
28	D28	D28	D28
29	D29	D29	D29
30	D30	D30	D30
31	D31	D31	D31
32	CS1#	CE2#	CE2#
33	VS1#	VS1#	VS1#
34	IORD#	IORD#	IORD#
35	IOWR#	IOWR#	IOWR#

36	VCC	WE#	WE#
37	READY	INTRO	IREQ
38	VCC	VCC	VCC
39	CSEL#	GND	GND
40	VS2#	VS2#	VS2#
41	RESET#	RESET	RESET
42	IORDY	WAIT#	WAIT#
43	NC	INPACK#	INPACK#
44	VCC	REG#	REG#
45	DASP#	BVD2	SPKR#
46	PDIAG#	BVD1	STSCHG#
47	D24	D24	D24
48	D25	D25	D25
49	D26	D26	D26
50	GND	GND	GND

5.4.4. Hard Disk

The following table shows the functions of each pin of the Hard Disk connector, which can only operate in True IDE mode:

Pin	TRUE IDE function	Pin	TRUE IDE function
1	RSTIO#	2	GND
3	D23	4	D24
5	D22	6	D25
7	D21	8	D26
9	D20	10	D27
11	D19	12	D28
13	D18	14	D29
15	D17	16	D30
17	D16	18	D31
19	GND	20	NC
21	NC	22	GND
23	IOWR#	24	GND
25	IORD	26	GND
27	IOCHRDY	28	CSEL
29	NC	30	GND
31	IRQ	32	IOCS16
33	A1	34	NC
35	A0	36	A2
37	CS0	38	CS1#
39	HD_ACTIVITY	40	GND
41	VCC	42	VCC
43	GND	44	NC

5.5. JTAG / Debugging

A JTAG interface is required both for debug purposes and for boundary scan testing of the UNC20 module during the manufacturing process.

The address lines ADDR[5..9] from the processor are multiplexed with the 5 JTAG lines. The selection is done via the LEDLNK/SEL signal. JTAG is active when the LED, connected to LEDLNK/SEL, is shorted to ground. This is achieved by inserting a jumper (J1) on the base board.

Pin	A	Description when inserted	Factory default
▌1		JTAG active	Not inserted
▌2			

Jumper settings for J1 ▌= connected pins

To activate the JTAG interface, the jumper has to be inserted.

NOTE: the CPLD requires address lines 5 to 9, therefore when J1/1-2 is inserted it will not be possible to access CompactFlash cards.

There are 3 connectors available on the base board for accessing JTAG on the UNC20 module: firstly, the ARM-defined 20-pin header (X4); secondly, the 8-pin header for FS Forth-Systeme's JTAG Booster connected to UNC (X3); thirdly, the Parallel Port JTAG adapter (PPJ) is implemented on the board using a buffer together with a standard 25-pin parallel port connector (DB25P).

There is a fourth JTAG connector (X7) for accessing the CPLD. This is also an 8-pin header for FS Forth-Systeme's JTAG Booster.

5.5.5. Parallel Port JTAG Adapter

The parallel port JTAG adapter allows for a direct connection between the host PCs parallel port and the JTAG pins of the UNC20. This allows a number of low-cost Development Tools to be used without additional hardware.

A 25-pin male D-type connector (X5) is provided for this purpose.

Pin	Parallel Function	JTAG Function
2	D0	TDI
3	D1	TMS
4	D2	TCK
5	D3	TRST#
7	D5	Reset#
8	D6	Port Sense
10	ACK#	Port Sense
12	PE	TDO
15	ERROR#	VCC sense

A parallel cable for connecting the host PC's parallel port to X5 is provided with the UNC20 Developer's Kit.

5.5.6. JTAG Booster

FS Forth-Systeme offers a JTAG Booster which allows accelerated programming of the UNC20 on-board Flash. An 8-pin header (X3) is provided for connecting the JTAG Booster.

It also allows the CPLD to be re-programmed, if connected to X7.

Note that the JTAG Booster is not part of the standard UNC20 Developer's Kit.

5.5.7. ARM-standard JTAG Connector

The JTAG connector is a 20-pin header as defined by ARM Ltd. and can be used for connecting a range of development tools such as ARM's Multi-ICE, Abatron's BDI2000 and EPI's JEENI.

Pin	Function	Pin	Function
1	3.3V	**2**	3.3V
3	TRST#	**4**	GND
5	TDI	**6**	GND
7	TMS	**8**	GND
9	TCK	**10**	GND
11	RTCK	**12**	GND
13	TDO	**14**	GND
15	SRST#	**16**	GND
17	N/C	**18**	GND
19	N/C	**20**	GND

5.6. Peripherals

An 8-bit data bus and 10-bit address bus are provided for connecting external peripherals to the UNC20. Two individually programmable chip selects (CS3# and CS4#) and an OE# (Output Enable) and WE# (Write Enable) signal allow a vast range of 8-bit peripherals to be connected directly to the UNC20 without any glue logic. In addition, the UNC20 module has two 8-bit General Purpose I/O ports (GPIO). Some of these 16 GPIO pins are already used on the base board. The following table gives an overview, showing those signals which are free to be used by additional hardware.

Port A	Use	Port C	Use
A0	Free	**C0**	Push-button (free if don't use button)
A1	Free	**C1**	Serial_1_CTS
A2	Free	**C2**	I2C (SDA)
A3	Free	**C3**	Serial_1_RxD
A4	LED (free if jumper removed)	**C4**	Push-button (free if don't use button)
A5	Free	**C5**	Serial_1_RTS (free if don't use Serial_1)
A6	LED (free if jumper removed)	**C6**	I2C (SCL)
A7	Free	**C7**	Serial_1_TxD (free if don't use Serial_1)

5.6.8. Switches and LEDs

The base board contains 2 push-buttons which can be used by the application to input information. Also 2 user LEDs are assembled to signal output activity for the applications. The 2 LEDs and 2 switches are connected to 4 GPIO pins. Since the LEDs use Port A4 and Port A6, which might be required by other peripherals, they can be disabled by removing J1/5-6.

Pin	A	Description when inserted	Factory default
▌5		LEDs active	Inserted
▌6			

Jumper settings for J1 ▌= connected pins

There is one LED that represents the Hard Disk activity.

A fourth LED denotes power on.

5.6.9. Access to UNC20 Pins

Users can freely access the UNC20 pins by means of the 42-pin header X6, which is not assembled. Pin-out of X6 is described below.

Pin	Function	Pin	Function
1	ADDR4	**2**	3.3V
3	ADDR5	**4**	CS4#
5	ADDR6	**6**	CS3#
7	ADDR7	**8**	OE#
9	ADDR8	**10**	WE#
11	ADDR9	**12**	ADDR3
13	PortA0	**14**	ADDR2
15	PortA1	**16**	ADDR1
17	PortA2	**18**	ADDR0
19	PortA3	**20**	D0
21	PortA4	**22**	D1
23	PortA5	**24**	D2
25	PortA6	**26**	D3
27	PortA7	**28**	D4
29	PortC0	**30**	D5
31	CTS1 (PortC1)	**32**	D6
33	SDA_I2C	**34**	D7
35	RxD1 (PortC3)	**36**	RESET#
37	PortC4	**38**	TxD1 (PortC7)
39	RTS1 (PortC5)	**40**	GND
41	SCL_I2C	**42**	GND

5.7. Power Supply and Reset

The external main power supply is provided by a standard plugable power supply (e.g. Friwo MPP15-FW7555M/06) which is connected to the power socket (X8) on the base board.

The base board provides the power supply for the UNC20 module and all onboard devices such as the serial line driver. The external power supply for the board is 5V DC. There is no power switch available. The board is switched on, by plugging in the power supply. A red LED on the base board denotes power on. A reset button is also provided.

5.7.10. Voltage Requirements

For the UNC20 module only a single 3.3V DC power supply is needed. This is generated on the base board.

6. UNC20 Connector

Pin	Signal	Type	Description
1	ADDR4	O	
2	ADDR5/TCK	O/I	**ADDR[5..9] are multiplexed with JTAG functionality – controlled by LEDLNK/SEL signal**
3	ADDR6/TMS	O/I	
4	ADDR7/TDI	O/I	
5	ADDR8/TDO	O/O	
6	ADDR9/TRST#	O/I	
7	PORTA0	I/O	
8	PORTA1	I/O	
9	PORTA2	I/O	
10	PORTA3	I/O	
11	PORTA4	I/O	
12	PORTA5	I/O	
13	PORTA6	I/O	
14	PORTA7	I/O	
15	PORTC0	I/O	
16	PORTC1	I	RS232 CTS
17	PORTC2	O	Hardwired as I2C data signal (SDA)
18	PORTC3	I	RS232 RxD
19	PORTC4	I/O	
20	PORTC5	O	RS232 RTS
21	PORTC6	I/O	Hardwired as I2C clock signal (SCL)
22	PORTC7	O	RS232 TxD
23	+3.3V	P	Power Supply
24	GND	P	Ground Connection
25	RSTIN#	I	Reset Input

26	TPIP	I	Ethernet Input+
27	TPIN	I	Ethernet Input-
28	TPOP	O	Ethernet Output+
29	TPON	O	Ethernet Output-
30	LEDLNK/SEL	O	Ethernet Activity LED; ADDR/JTAG Selection: JTAG active when grounded
31	USB-	I/O	USB differential data negative
32	USB+	I/O	USB differential data positive
33	DATA31	I/O	Data line D7
34	DATA30	I/O	D6
35	DATA29	I/O	D5
36	DATA28	I/O	D4
37	DATA27	I/O	D3
38	DATA26	I/O	D2
39	DATA25	I/O	D1
40	DATA24	I/O	D0
41	ADDR0	O	Address Line
42	ADDR1	O	Address Line
43	ADDR2	O	Address Line
44	ADDR3	O	Address Line
45	WE#	O	Write Enable
46	OE#	O	Output Enable
47	CS3#	O	Chip Select 3
48	CS4#	O	Chip Select 4

The UNC20 connector is based on a standard DIP48 socket.